28F016XS
SPECIFICATION UPDATE

Release Date: November 1996

Order Number 297553-007

The 28F016XS may contain design defects or errors known as errata. Characterized errata that may cause the 28F016XS's behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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Germany 44-0-1793-421-333 other Countries 708-296-9333

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REVISION HISTORY

Date of Revision	Version	Description
10/24/94	-001	Document includes all known errata to date (Original Version)
01/23/95	-002	Added: Device Version Numbers 01H and 02H V_{CC} Deep Power-Down Current Queueable Operation Delay after Power-Up and Exit from Sleep, Power-Down, or Reset WE# and CE_X# Pulse Width High Requirements after Issuing Queueable Commands Page Buffer Programming Completion with Command Error Indication and Invalid Device Operations WP# Control V_{PP} Read Current Deleted: Status Register Reads Updated: AC Characteristics for WE# and CE_X#-Controlled Page Buffer Write Operations Erase Interruptability Obsoleted: Page Buffer Reads Non-Serviced Erase Suspend Command AC Read Timing Waveform
02/22/95	-003	Added: Device Version Number 03H Deleted: AC Characteristics for WE# and CE_X#-Controlled Page Buffer Write Operations Page Buffer Reads Page Buffer Programming Erase Interruptability Updating Global Status Register Bits 0 and 1 Active Current Consumption during Sleep Mode V_{PP} Read Current BYTE# Level during Deep Power-Down Mode RP# High to CLK High Word/Byte Write Performance Updated: Operation Delay after Power-Up and Exit from Power-Down or Reset WE# and CE_X# Pulse Width High Requirements after Issuing Commands Completion with Command Error Indication Non-Service Erase Suspend Command WP# Control Obsoleted: Completion with Command Error Indication WP# Control

REVISION HISTORY, Continued

Date of Revision	Version	Description
06/28/95	-004	Added: Device Version Number 04H 3.3V V_{CC} Requirement for Optimal Power Savings V_{PP} Voltage Tolerance Requirement for Program/Erase Operations at 3.3V V_{CC} RP# Input Level Control at 5V V_{CC} Non-Serviced Block Erase with Stuck Block Status Register Erase Operation with Block Lock Notification Deleted: Power-Up and Reset Timings Updated: V_{CC} Standby and Deep Power-Down Currents Obsoleted: 3.3V V_{CC} Requirement for Optimal Power Savings Non-Serviced Block Erase with Stuck Block Status Register Erase with Block Lock Notification
07/01/96	-005	This is the new format for the Specification Update document. It contains all identified errata published prior to this date.
08/09/96	-006	Added 5V/3V CE# Controlled Write Timings (t_{AVAV}, t_{ELEH}) V_{PP} Erase Suspend Current (I_{PPES}) V_{CC} Tolerance Requirement Obsoleted WE# and CE_X# Pulse Width High Requirements after Issuing commands. V_{PP} Voltage Tolerance Requirement for Program/Erase Operations at 3.3V V_{CC}. RP# Input Level Control at 5V V_{CC} Operation Delay after Power-Up and Exit from Power-Down Reset. Update: V_{CC} Standby and Deep Power-Down Currents
11/11/96	-007	Updated: Device Version Number Device Version Number and FPO Number Relationship Table

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This is the seventh release of the 28F016XS Specification Update. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published.

Functional descriptions for this product are found in the *28F016XS 16-Mbit (1 Mbit x 16, 2 Mbit x 8) Synchronous Flash Memory Datasheet*.

Affected Documents/Related Documents

Title	Order
28F016XS 16-Mbit (1 Mbit x 16, 2 Mbit x 8) Synchronous Flash Memory Datasheet	290532
16-Mbit Flash Product Family User's Manual	297372

Nomenclature

Errata are design defects or errors. These may cause the 28F016XS's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation.

Documentation Changes include typos, errors, or omissions from the current published specifications.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the product's user documentation (datasheets, manuals, etc.).

SUMMARY TABLES OF CHANGES

The following tables indicate the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the *28F016XS 16-Mbit (1 Mbit x 16, 2 Mbit x 8) Synchronous Flash Memory Datasheet*. Intel may fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Number	Device Version Numbers							Page	Status	Errata
	00	01	02	03	04	05	06			
9600001	X	X	X	X	X	X		9	Doc	V_{CC} Standby and Deep Power-Down Currents
9600002	X	X	X	X				10	Fixed	3.3V V_{CC} Requirement for Optimal Power Savings
9600003	X	X	X	X	X	X		11	Fixed	V_{PP} Voltage Tolerance Requirement for Program/Erase Operations at 3.3V V_{CC}
9600004	X	X	X	X	X	X		11	Fixed	RP# Input Level Control at 5V V_{CC}
9600005	X	X	X	X	X	X		12	Fixed	WE# and CE_X# Pulse Width High Requirements after Issuing Commands
9600006	X	X	X	X	X	X		13	Fixed	Operation Delay after Power-Up and Exit from Power-Down or Reset
9600007	X	X						14	Fixed	Completion with Command Error Indication
9600008	X							17	Fixed	Non-Serviced Erase Suspend Command
9600009	X	X	X	X				20	Fixed	Non-Serviced Block Erase with Stuck Block Status Register
9600010	X	X	X	X				20	Fixed	Erase Operation with Block Lock Notification
9600011	X	X	X					21	Fixed	WP# Control
9600012	X	X	X	X	X	X		21	Doc	SFI Configuration Table
9600013	X							22	Fixed	AC Read Timing Waveform

Specification Changes

Number	Device Version Number							Page	Status	Specification Change
	00	01	02	03	04	05	06			
001							X	24	Doc	V_{CC} Tolerance Requirement
002							X	24	Doc	5V/3VCE# Controlled Write Timings
003							X	25	Doc	V_{CC} Standby and Deep Power-Down Currents
004							X	26	Doc	V_{PP} Erase Suspend Current (I_{PPES})

Specification Clarifications

Number	Device Version Number							Page	Status	Specification Clarifications
								27		None in this Specification Update revision.

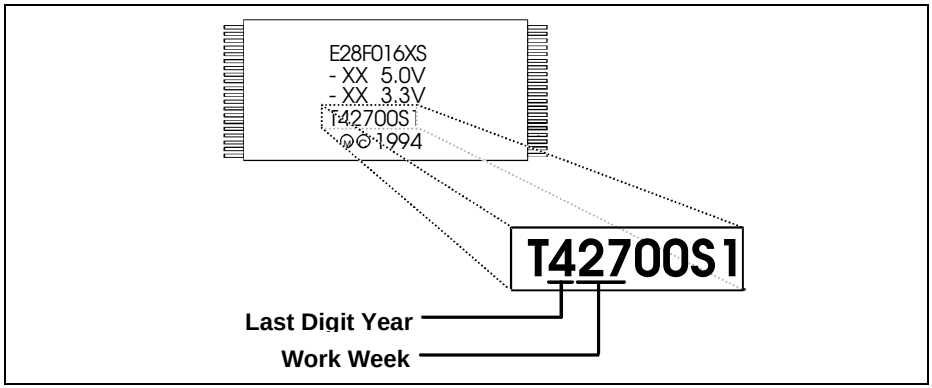
Documentation Changes

Number	Document Revision	Page	Status	Documentation Changes
		27		None in this Specification Update revision.

IDENTIFICATION INFORMATION

Markings

The Finished Processing Order (FPO) number identifies the device's testing date. The FPO number correlates to a specific Device Version Number, as illustrated below:



FPO Number Location and Clarification

Device Version Number and FPO Number Relationship to Specific Component Stepping

Stepping	Device Version Number(1)	FPO Number	
		Work Week	Year
A-0	00H	≤34	1994
A-1	01H	≥35(2)	1994
	02H	≥01	1995
	03H	≥14	1995
A-2	04H	≥31	1995
A-4	05H	≥09	1996
B-1	06H	≥28	1996

NOTES:

1. Device Version Numbers are based on continuous improvements made in manufacturing and testing of the device and represent the current material shipped.
2. Components with FPO number U4400052 are from the A-0 Stepping. They are **not** A-1 material, as the Work Week indicates.

ERRATA

9600001. V_{CC} Standby and Deep Power-Down Currents

PROBLEM: The V_{CC} standby (I_{CCD}) and deep power-down (I_{CCD}) currents exceed the maximum specification values published in the *28F016XS 16-Mbit (1 Mbit x 16, 2 Mbit x 8) Synchronous Flash Memory Datasheet*.

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C
3/5# Pin Set High for 3.3V Operations

Symbol	Parameter	Max Spec	Max New	Test Conditions
I_{CCS}	V_{CC} Standby Current	130 µA	350 µA(1) 130 µA(2)	V_{CC} = V_{CC} Max, CE_0#, CE_1#, RP# = V_{CC} ± 0.2V BYTE#, WP#, 3/5# = V_{CC} ± 0.2V or GND ± 0.2V
I_{CCD}	V_{CC} Deep Power-Down Current	5 µA	350 µA(1) 10 µA(2)	RP# = GND ± 0.2V BYTE# = V_{CC} ± 0.2V or GND ± 0.2V

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0°C to +70°C
3/5# Pin Set Low for 5V Operations

Symbol	Parameter	Max	Max New	Test Conditions
I_{CCS}	V_{CC} Standby Current	130 µA	350 µA(1) 130 µA(2)	V_{CC} = V_{CC} Max, CE_0#, CE_1#, RP# = V_{CC} ± 0.2V BYTE#, WP#, 3/5# = V_{CC} ± 0.2V or GND ± 0.2V
I_{CCD}	V_{CC} Deep Power-Down Current	5 µA	350 µA(1) 10 µA(2)	RP# = GND ± 0.2V BYTE# = V_{CC} ± 0.2V or GND ± 0.2V

NOTES:
1. These specification values apply to components with a Device Revision Code of 00H.
2. These specification values apply to components with Device Revision Codes 01H, 02H, 03H, 04H and 05H.

Upon entering standby and/or deep power-down mode(s), a current surge with a peak amplitude of 200 µA may occur for a duration of up to 30 seconds. This surge will only happen at most once while in one of these two modes. These errata only affect components listed in the Affected Products section.

Please note that the Reset functionality of the RP# pin is preserved, and it should still be used for the following purposes:

- Write Protection during system power transitions
- Device Reset to read array mode upon exit from deep power-down mode
- Termination of Write State Machine operations upon entry into deep power-down mode

IMPLICATION: The increased current specifications may have an impact on power supply loading or battery life.

WORKAROUND: Ensure that system power supply and/or battery is sufficient to meet the increased current requirements.

STATUS: Plans to fix this erratum are under evaluation. Refer to Summary Table of Contents to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H, 03H, and 04H are affected. (04H eliminates the possibility of a deep power-down current surge). Note that I_{CCS} specifications have returned to datasheet values and I_{CCD} current specifications have been increased for devices with Device Version Numbers 01H, 02H, 03H, 04H, and 05H.

9600002. 3.3V V_{CC} Requirement for Optimal Power Savings

PROBLEM: When operating at 3.3V V_{CC}, the read voltage (V_{CC}) must ramp to 3.2V or greater (maximum voltage 3.6V) to achieve the published standby current (I_{CCS}) specifications. Once the read voltage crosses this voltage threshold, the V_{CC} tolerance requirement returns to the datasheet specification of 3.3V ± 0.3V.

IMPLICATION: If the read voltage (V_{CC}) does not ramp to 3.2V or greater (maximum voltage 3.6V), the increased current consumption may have an impact on power supply loading or battery life.

WORKAROUND: Ramp the read voltage (V_{CC}) 3.2V or greater (maximum voltage 3.6V).

STATUS: This erratum has been fixed. Refer to Summary Table of Contents to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H, 03H and 04H are affected.

9600003. V_{PP} Voltage Tolerance Requirement for Program/Erase Operations at 3.3V V_{CC}

PROBLEM: When programming or erasing data at 3.3V V_{CC} and 5V V_{PP}, the program voltage (V_{PP}) is restricted to 5V ± 0.25V (5%).

IMPLICATION: V_{PP} voltage restriction when programming or erasing data at 3.3V V_{CC} and 5V V_{PP} is impacted.

WORKAROUND: Restrict programming voltage to 5V ± 0.25V when programming or erasing data at 3.3V V_{CC} and 5V V_{PP}.

STATUS: Plans to fix this erratum are under evaluation. Refer to Summary Table of Contents to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H, 03H, 04H, and 05H are affected.

9600004. RP# Input Level Control at 5V V_{CC}

PROBLEM: The device's RP# input pin must be driven to a minimum V_{IH} voltage of 3.0V when operating at 5V V_{CC}. Therefore, system RP# control logic, if implemented, must drive V_{OH} greater than 3.0V. If such logic is not employed, RP# should be tied to V_{CC} ± 0.2V.

IMPLICATION: Failure to drive RP# to 3.0V could cause the device to stay in reset.

WORKAROUND: When operation at 5V V_{CC}, drive the device's RP# input pin to a minimum V_{IH} voltage of 3.0V.

STATUS: Plans to fix this erratum are under evaluation. Refer to Summary Table of Contents to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H, 03H, 04H, and 05H are affected.

9600005. WE# & CE_X# Pulse Width High Requirements after Issuing Commands

PROBLEM: The WE# and CE# pulse width high requirements that deviate from the *28F016XS 16-Mbit (1 Mbit x 16, 2 Mbit x 8) Synchronous Flash Memory Datasheet* are shown below. The t_{WHWL} and t_{EHEL} specification changes only apply when writing to the device immediately following the completion of issuing the following commands:

- Word/Byte Write (40H/10H)
- Block Erase (20H)
- Lock Block (77H)
- Device Configuration (96H)
- Upload Status Bits (97H)

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Versions		28F016XS-20		28F016XS-25	
Symbol	**Parameter**	**Min Spec**	**Min New**	**Min Spec**	**Min New**
t_{WHWL}	WE# Pulse Width High	15 ns	45 ns(1)	15 ns	45 ns(1)
t_{EHEL}	CE# Pulse Width High	15 ns	45 ns(1)	15 ns	45 ns(1)

V_{CC} = 5V ± 0.5V, T_A = 0°C to +70°C

Versions		28F016XS-15		28F016XS-20	
Symbol	**Parameter**	**Min Spec**	**Min New**	**Min Spec**	**Min New**
t_{WHWL}	WE# Pulse Width High	15 ns	30 ns(1)	15 ns	30 ns(1)
t_{EHEL}	CE# Pulse Width High	15 ns	30 ns(1)	15 ns	30 ns(1)

NOTE:

1. These new specification values only apply when writing to the device immediately following the completion of issuing a command listed earlier.

IMPLICATION: Write operations are impacted.

WORKAROUND: Adhere to modified AC write specifications when issuing software sequence outlined in the description section.

STATUS: Plans to fix this erratum are under evaluation. Refer to Summary Table of Contents to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H, 03H, 04H, and 05H are affected.

9600006. Operation Delay after Power-Up and Exit from Power-Down or Reset

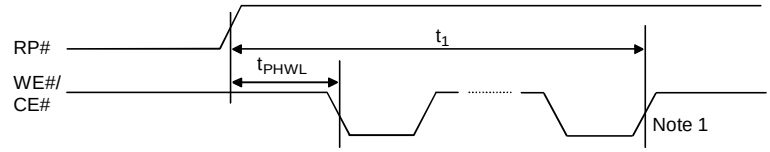
PROBLEM: With the program/erase voltage (V_{PP}) at 5V, the internal V_{PP} detector may not stabilize for up to 5 µs (illustrated by t_1, in the figure below) after RP# transitions inactive (high). This causes an invalid V_{PP} Level bit indication when reading the Block Status Registers and termination of program, erase or lock block operations due to invalid device V_{PP} error detection. Affected operations include Word Write (40H/10H), Block Erase (20H) and Lock Block (77H).

Note that this erratum only affects systems operating at 5V V_{PP}.

IMPLICATION: The 5V V_{PP} power-up/reset time delay to first program or erase operation is impacted.

WORKAROUND: Upon reset, power-up, or wake-up from software sleep or hardware deep power-down, allow 5 µs (t_1) before initiating a Write/Erase command (as listed earlier) or reading the V_{PP} Level bit of the Block Status Registers (BSR.1). The figure, *Operation Delay after Power-Up and Exit from Power-Down or Reset*, illustrates this timing requirement (t_1) in more detail.

Operations are initiated by the device on the rising (trailing) edge of the last WE#/CE# pulse in the command sequence. For example, when performing WE#-Controlled Writes, two-cycle command operations such as word/byte write or erase are initiated on the rising edge of the WE# pulse corresponding to the Address/Data or Confirm command. Similarly, when performing CE#-Controlled Writes, operations are initiated on the last rising CE# edge of the command sequence.



NOTE:

1. This rising edge of WE#/CE# represents the completion of the command sequence—i.e., the time at which the command is latched into the WSM and the internal automation is initiated.

Operation Delay after Power-Up and Exit from Power-Down or Reset

STATUS: Plans to fix this erratum are under evaluation. Refer to Summary Table of Contents to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H, 03H, 04H, and 05H are affected.

9600007. Completion with Command Error Indication

PROBLEM: Systems in which software, after initiating device automation, writes another command(s) to the device before automation completes may initiate unintended device operations.

IMPLICATION: Designs that could encounter this condition include the following:

- Systems that poll for automation completion using the Extended Status Registers (thereby writing the Read Extended Status Register command after initiating automation)
- Systems that write the Read Compatible Status Register command after initiating device automation and before reading the Compatible Status Register (This command is actually unnecessary as the device, after receiving commands or command sequences, automatically transitions to a mode where it outputs Compatible Status Register data when read.)
- Systems that use the Erase Suspend command

These unintended operations will produce an invalid command error indication. A command error is indicated by a “1” in the following Status Register bits:

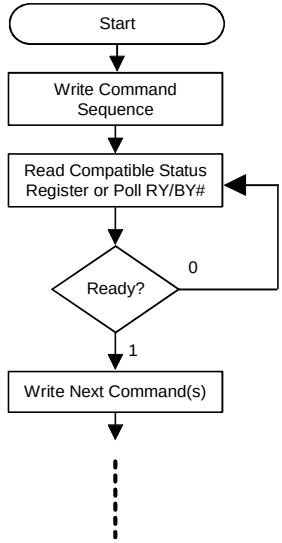
Compatible Status Register	Bit 5: Erase Status
	Bit 4: Data-Write Status
Global Status Register	Bit 5: Device Operation Status
Block Status Register (Block 0)	Bit 5: Block Operation Status

This erratum only affects components listed in the Affected Products section.

WORKAROUND: The following options listed below outline possible corrective actions required to avoid this erratum. (Either of the options will eliminate this erratum.)

Option 1: Polling for "Ready" Indication

Systems that poll the RY/BY# pin or WSMS bit (CSR.7) for "Ready" indication before writing another command to the device will not encounter this erratum. This is illustrated in the *Example System Software Flowchart, etc*. figure below, and in flowcharts 11-1 and 11-2 (without erase suspend) of the *16-Mbit Flash Memory Product Family User's Manual*.



NOTE:
System software does not write the Read Compatible Status Register command before reading status register data.

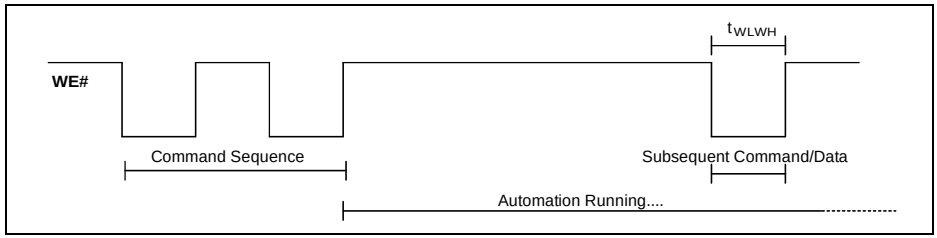
Example System Software Flowchart That Will Not Encounter "Completion with Command Error" Condition

Option 2: WE# Pulse Width Restrictions

For WE#–Controlled Write Operations, a WE# pulse width defined by the ranges of parameter t_{WLWH},in the table below, will result in a system that does not exhibit this erratum. (Note: timings are also bounded by specifications in the device datasheet). When performing CE#–Controlled Write Operations, this restriction equally applies to the CE# pulse width (t_{ELEH}).

WE# and CE# Specifications That Will Not Cause the "Completion with Command Error" Condition

V_{CC} Supply Voltage	t_{WLWH}	t_{ELEH}
5V	<75 ns	<75 ns
3.3V	<100 ns	<100 ns



Timing Waveform Showing Specification Ranges That Will Not Cause the "Completion with Command Error" Condition

STATUS: This erratum has been fixed. Refer to Summary Table of Contents to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H and 01H are affected.

9600008. Non-Serviced Erase Suspend Command

PROBLEM: If an Erase Suspend command is issued late in the Erase algorithm, it will not be recognized by 28F016XS components listed in the Affected Devices section, and erase will complete. This Erase Suspend command will **not** be discarded.

IMPACT: The following conditions are affected by this unserviced Suspend command:

A. If another Erase command is issued at some time later, the device then assumes that the pending Suspend request is still valid and will automatically Suspend the current Erase.

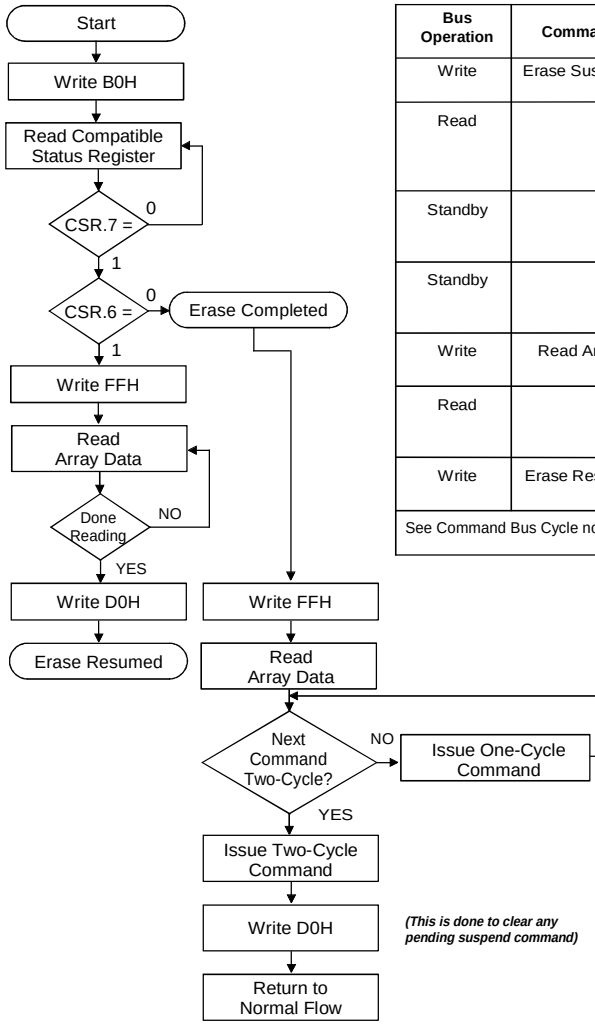
B. If any queueable command is in the command queue waiting for execution while another queueable command is in progress, the Write State Machine will suspend its operation after completing the current command. (Refer to the *16-Mbit Flash Product Family User's Manual*, Section 11-1 for the queueable command list.)

Note that the device will not service the Suspend command if it is powered-down (RP# transitioning low) prior to either condition A or B.

WORKAROUND: A software workaround to this erratum inserts a redundant Resume command (D0H) immediately following any Two-Cycle Command (Word Write, Block Erase, Lock Block, or Upload Status Bits) in the Erase Suspend flowcharts. Modified Erase Suspend to Read Array flowcharts (Figures 11-3 and 11-12 of the *16-Mbit Flash Memory Product Family User's Manual*) detailing this workaround are shown in *the Erase Suspend to Read Array with Compatible Status Register* and *Erase Suspend to Read Array with Extended Status Register* figures, which follow. This erratum results in the *Erase Suspend with Compatible Status Register* flowchart being incompatible with the 28F008SA *Erase Suspend* flowchart.

STATUS: This erratum has been fixed. Refer to Summary Table of Contents to determine the affected stepping.

AFFECTED PRODUCTS: All components with Device Version Number 00H are affected.

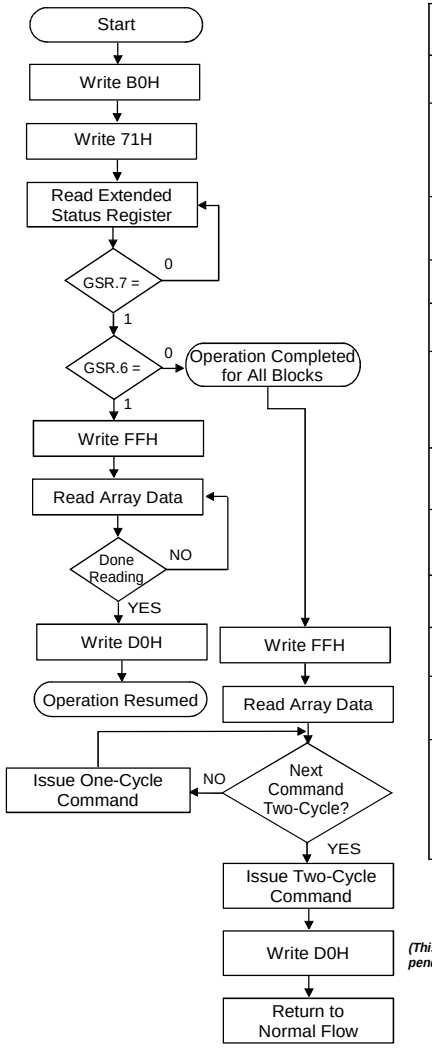


Bus Operation	Command	Comments
Write	Erase Suspend	D = B0H A = X

Read		Q = CSRD
		Toggle CE_0 #, CE_1 # or OE# to Update CSRD.
		A = X

Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check CSR.6 1 = Erase Suspended 0 = Erase Completed
Write	Read Array	D = FFH A = X
Read		Q = AD Read must be from block other than the one suspended.
Write	Erase Resume	D = D0H A = X
See Command Bus Cycle notes for description of codes.		

Erase Suspend to Read Array with Compatible Status Register



Bus Operation	Command	Comments
Write	Read Extended Status Register	D = 71H A = X

Read (Note 1)		Q = BSRD
		Toggle CE_0 #, CE_1 # or OE# to Update BSRD.
		A = 2H (x8 Mode)
		A = 1H (x16 Mode)

Standby		Check BSR.7 1 = Block Ready 0 = Block Busy
Write	Erase Suspend	D = B0H A = X
Write	Read Extended Status Register	D = 71H A = X

Read		Q = GSRD
		Toggle CE_0 #, CE_1 # or OE# to Update BSRD.
		A = 4H (x8 Mode)
		A = 2H (x16 Mode)

Standby		Check GSR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check GSR.6 1 = Operation Suspended 0 = Operation Completed
Write	Read Array	D = FFH A = X
Read		Q = AD A = AA
Write	Operation Resume	D = D0H A = X

1. The address for the desired BSR to be read must be supplied on A_{20} - A_{17}.
2. Check BSR.7 of block to be read. This should be a block other than the one suspended, or queued for an operation.

See Command Bus Cycle notes for description of codes.

(This is done to clear any pending suspend command)

Erase Suspend to Read Array with Extended Status Register

9600009. Non-Serviced Block Erase with Stuck Block Status Register

PROBLEM: If software polls the BS bit of the Block Status Register for block erase completion (BSR.7 = 1) and immediately issues a subsequent block erase command sequence before the WSMS bit of the Compatible Status Register or Global Status Register indicate "Ready" (CSR.7/GSR.7 = 1), the device may not service the subsequent erase operation. This scenario also causes the BS bit of the subsequent block to remain in the "Busy" state (BSR.7 = 0).

IMPLICATION: Block erase operations may be left unserviced.

WORKAROUND: To avoid this erratum, system software should poll CSR.7 (as shown in Figure 11-2 of the *16-Mbit Flash Product Family User's Manual*) or GSR.7, instead of BSR.7, to determine the completion of a block erase operation before issuing subsequent block erase commands.

STATUS: This erratum has been fixed. Refer to Summary Table of Contents to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H and 03H are affected.

9600010. Erase Operation with Block Lock Notification

PROBLEM: A Block Erase (20H) operation with the block address on an odd word boundary may unintentionally lock the block targeted for erasure.

IMPLICATION: Block erase operation may cause unintentional block locking.

WORKAROUND: This erratum can be avoided by using an even word boundary (A_1 = "0") when selecting the desired block for erase. Otherwise, WP# should be driven inactive (WP# = "1") to avoid permanent block locking in system.

STATUS: This erratum has been fixed. Refer to Summary Table of Contents to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H and 03H are affected.

9600011. WP# Control

DESCRIPTION:

Block erase can prematurely terminate as the result of hardware RP# activation or V_{CC} transition outside of the normal operating range. In these non-standard scenarios, there exists a small probability that the block's lock-bit will become set, locking the block even though WP# is active (low).

IMPLICATION: Systems may inadvertently lock blocks. The system will not be able to write or erase locked blocks while WP# is held low.

WORKAROUND: System software can detect premature termination of block erase by executing the Upload Status command on device power-up. If both BSR.5 and GSR.5 are set, indicating premature block erase termination, the system should re-attempt erase with WP# inactive (high).

System hardware should be designed to either control WP# (both active and inactive levels must be supported) or should set WP# inactive at all times. Setting WP# always-active (i.e., connecting it to GND) is not recommended as this configuration will not enable recovery from inadvertent lock during premature block erase termination.

STATUS: This erratum has been fixed. Refer to Summary Table of Contents to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, and 02H are affected.

9600012. SFI Configuration Table

PROBLEM: 28F016XS components are not tested at speeds greater than 50 MHz. Therefore, the 28F016XS-15 SFI Configuration number 4 is valid for CLK input frequencies up to 50 MHz (as opposed to the datasheet value of 66 MHz). Testing methodologies are being developed for speeds greater than 50 MHz.

Below is a revised SFI Configuration Table (Section 4.9 of the *28F016XS 16-Mbit (1 Mbit x 16, 2 Mbit x 8) Synchronous Flash Memory Datasheet*):

SFI Configuration	28F016XS-15 Frequency (MHz)	28F016XS-20 Frequency (MHz)	28F016XS-25 Frequency (MHz)
4	50 (and below)	50 (and below)	40 (and below)
3	50 (and below)	37.5 (and below)	30 (and below)
2	33 (and below)	25 (and below)	20 (and below)
1	16.7 (and below)	12.5 (and below)	10 (and below)

IMPLICATION: This erratum limits the maximum input CLK frequency.

WORKAROUND: Adhere to the modified SFI Configuration Table.

STATUS: Under evaluation.Affected Products: All components with Device Version Numbers 00H, 01H, 02H, 03H, 04H and 05H are affected. Refer to Summary Table of Contents to determine the affected steppings.

9600013. AC Read Timing Waveform

PROBLEM: An additional wait-state is required between consecutive Same-A_1 accesses for components listed in the Affected Products section.

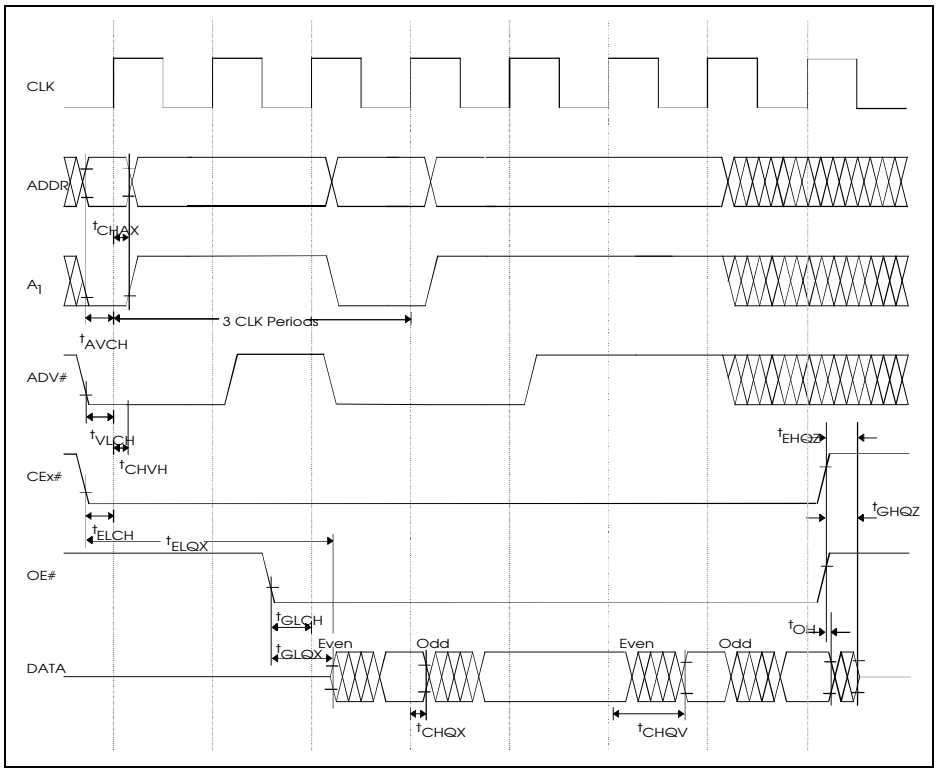
IMPLICATION: This erratum effects consecutive pipelined read accesses.

WORKAROUND: A new Same-A_1 (same bank) address cannot be placed on the bus until after the rising clock edge upon which data for the previous Same-A_1 (same bank) access is driven out of the 28F016XS flash memory device. This rising CLK edge will occur a number of clock cycles equal to the SFI Configuration setting after latching the address from the previous Same-A_1 access. Addresses are latched upon sensing ADV# low in conjunction with a rising CLK edge.

The Read Timing Waveform, which follows, illustrates a modified version of the read timing waveform, Figure 11 in the *28F016XS 16-Mbit (1 Mbit x 16, 2 Mbit x 8) Synchronous Flash Memory Datasheet*, which illustrates this burst access sequence described in the previous paragraph. Similarly, this condition applies to all SFI Configurations.

STATUS: Plans to fix this erratum are under evaluation. Refer to Summary Table of Contents to determine the affected stepping.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H are affected.



Read Timing Waveform (SFI Configuration = 2, Alternate-Bank Access)

SPECIFICATION CHANGES

001. V_{CC} Tolerance Requirement

PROBLEM: When operating the 28F016XS-015 or the 28F016XS-020 devices, V_{CC} should be varied no more than 5%. This specification change applies only to the 28F016XS-015 and the 28F016XS-020 line items.

IMPLICATION: When operation the 28F016XS-015 or the 28F016XS-020 in the 3.3V V_{CC} range, V_{CC} must not vary more than 3.3V $\pm$ 0.15. Likewise, when operating the 28F016XS-015 or the 28F016XS-020 in the 5V V_{CC} range, V_{CC} must not vary more than 5V $\pm$ 0.25.

WORKAROUND: Systems using the 28F016XS-015 or the 28F016XS-020 should implement power supplies that are accurate to within 5% for the V_{CC} supply.

STATUS: This is a permanent specification change. Refer to Summary Table of Contents to determine the affected steppings.

AFFECTED PRODUCTS: All 28F016XS-015 and 28F016XS-020 components with Device Version Number 06H are affected.

002. 5V/3V CE# Controlled Write Timings

PROBLEM: Two CE#-controlled write parameter requirements that deviate from the *28F016XS 16-Mbit (1 Mbit x 16, 2 Mbit x 8) Synchronous Flash Memory Datasheet* are shown below. Note that the t_{AVAV} and t_{ELEH} specification changes only apply when performing a CE# controlled write.

V_{CC} = 3.3V ± 0.15V, T_A = 0°C to +70°C

Versions		V_{CC} ± 5%	28F016XS-020		28F016XS-025	
		V_{CC} ± 10%			28F016XS-025	
Symbol	**Parameter**		**Min Spec**	**Min New**	**Min Spec**	**Min New**
t_{ELEH}	CE# Pulse Width Low		60 ns	65 ns	60 ns	65 ns
t_{AVAV}	Write Cycle Time		75 ns	80 ns	75 ns	80 ns

V_{CC} = 5V ± 0.25V, T_A = 0°C to +70°C

Versions		V_{CC} ± 5%	28F016XS-015		28F016XS-020	
		V_{CC} ± 10%			28F016XS-020	
Symbol	**Parameter**		**Min Spec**	**Min New**	**Min Spec**	**Min New**
t_{AVAV}	Write Cycle Time		60 ns	65 ns	60 ns	65 ns
t_{ELEH}	CE# Pulse Width High		45 ns	50 ns	45 ns	50 ns

IMPLICATION: Issuing CE# controlled writes

WORKAROUND: Adhere to modified AC write specifications when performing CE# controlled writes

STATUS: This is a permanent spec change. Refer to Summary Table of Contents to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Number 06H are affected.

003. V_{CC} Standby and Deep Power-Down Currents

PROBLEM: The V_{CC} standby (I_{CCD}) and deep power-down (I_{CCD}) currents exceed the maximum specification values published in the *28F016XS 16-Mbit (1 Mbit x 16, 2 Mbit x 8) Synchronous Flash Memory Datasheet*.

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C
3/5# Pin Set High for 3.3V Operations

Symbol	Parameter	Max Spec	Max New	Test Conditions
I_{CCS}	V_{CC} Standby Current	130 µA	350 µA(1) 130 µA(2)	V_{CC} = V_{CC} Max, CE_0#, CE_1#, RP# = V_{CC} ± 0.2V BYTE#, WP#, 3/5# = V_{CC} ± 0.2V or GND ± 0.2V
I_{CCD}	V_{CC} Deep Power-Down Current	5 µA	350 µA(1) 10 µA(2)	RP# = GND ± 0.2V BYTE# = V_{CC} ± 0.2V or GND ± 0.2V

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0°C to +70°C
3/5# Pin Set Low for 5V Operations

Symbol	Parameter	Max	Max New	Test Conditions
I_{CCS}	V_{CC} Standby Current	130 µA	350 µA(1) 130 µA(2)	V_{CC} = V_{CC} Max, CE_0#, CE_1#, RP# = V_{CC} ± 0.2V BYTE#, WP#, 3/5# = V_{CC} ± 0.2V or GND ± 0.2V
I_{CCD}	V_{CC} Deep Power-Down Current	5 µA	350 µA(1) 10 µA(2)	RP# = GND ± 0.2V BYTE# = V_{CC} ± 0.2V or GND ± 0.2V

NOTES:
1. These specification values apply to components with a Device Revision Code of 00H.
2. These specification values apply to components with Device Revision Codes 01H, 02H, 03H, 04H and 05H.

Upon entering standby and/or deep power-down mode(s), a current surge with a peak amplitude of 200 µA may occur for a duration of up to 30 seconds. This surge will only happen at most once while in one of these two modes. These errata only affect components listed in the Affected Products section.

Please note that the Reset functionality of the RP# pin is preserved, and it should still be used for the following purposes:

- Write Protection during system power transitions
- Device Reset to read array mode upon exit from deep power-down mode
- Termination of Write State Machine operations upon entry into deep power-down mode

IMPLICATION: The increased current specifications may have an impact on power supply loading or battery life.

WORKAROUND: Ensure that system power supply and/or battery is sufficient to meet the increased current requirements.

STATUS: This is a permanent specification change. Refer to Summary Table of Contents to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H, 03H, 04H, 05H and 06H are affected. (04H eliminates the possibility of a deep power-down current surge.) Note that I_{CCS} specifications have returned to datasheet values and I_{CCD} current specifications have been lowered for devices with Device Version Numbers 01H, 02H, 03H, 04H and 05H.

004. 3.3V and 5V V_{PP} DC Characteristics

PROBLEM: The following tables list DC characteristics that exceed the maximum specifications published in the *28F016XS 16-Mbit (1Mbit x 16) DRAM-Interface Flash Memory Datasheet*.

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C
3/5# Pin Set High for 3.3V Operations

Symbol	Parameter	Max Spec	Max New	Test Conditions
I_{PPES}	V_{PP} Erase Suspend Current	50 µA	200 µA	Block Erase Suspend

V_{CC} = 5V ± 0.5V, T_A = 0°C to +70°C
3/5# Pin Set Low for 5V Operations

Symbol	Parameter	Max Spec	Max New	Test Conditions
I_{PPES}	V_{PP} Erase Suspend Current	50 mA	200 uA	Block Erase Suspend

SPECIFICATION CLARIFICATIONS

There are no specification clarifications for this Specification Update revision.

DOCUMENTATION CHANGES

There are no documentation changes for this Specification Update revision.