28F400BX/BL
28F004BX/BL
28F200BX/BL
28F002BX/BL

SPECIFICATION UPDATE

Release Date: July 1996

Order Number 297187-008

The 28F400BX/BL, 28F004BX/BL, 28F200BX/BL and 28F002BX/BL may contain design defects or errors known as errata. Characterized errata that may cause the 28F400BX/BL, 28F004BX/BL, 28F200BX/BL and 28F002BX/BLs' behavior to deviate from published specifications are documented in this specification update.

Information in this document is provided in connection with Intel products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

The 28F400BX/BL, 28F004BX/BL, 28F200BX/BL and 28F002BX/BL may contain design defects or errors known as errata. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications before placing your product order.

* Third-party brands and names are the property of their respective owners.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect, IL 60056-7641

or call in North America 1-800-879-4683, Europe 44-0-1793-431-155, France 44-0-1793-421-777,

Germany 44-0-1793-421-333 other Countries 708-296-9333

Copyright © 1996, Intel Corporation

CONTENTS

REVISION HISTORY....1

PREFACE....2

SUMMARY TABLES OF CHANGES....4

IDENTIFICATION INFORMATION....6

ERRATA....7

SPECIFICATION CHANGES....16

SPECIFICATION CLARIFICATIONS....22

DOCUMENTATION CHANGES....23

REVISION HISTORY

Date of Revision	Version	Description
03/30/94	-001	Document includes all known errata to date: Erase Suspend, Prog/Erase Lock-Out Voltage, Pin #3, 3.3V V_{CC}, Write Timing.
03/30/94	-002	Extended Temp. Deep Power-Down Current added Column added to Summary Table categorizing each entry with an erratum type. Type information also added in parentheses after each title. Document description (above paragraph) revised. Affected material identification clarified for Erase Suspend and Program/Erase Lock-out Voltage 3.3V V_{CC} Operating Range reworded to clarify changes.
04/07/94	-003	2-Mbit parts removed from the list of parts affected by 3.3V V_{CC} Operating Range.
04/12/94	-004	Addendum for 120 ns speeds for 2/4-Mbit components added: see datasheet.
10/21/94	-005	Addendum for new operating temperature spec for 2/4-Mbit BL parts: see datasheet. Drawings in erratum Erase Suspend and Program/Erase Lock-Out Voltage redrawn to space space/memory.
12/01/94	-006	28F200/002BX mirrored die information added. Permanent spec change for Program/Erase Lock-out Voltage. Addendum for 120 ns speed 2/4-Mbit components removed. Addendum for new operating temperature specification for 2/4-Mbit BL parts removed.
10/20/95	-007	Specification change: I_{CCD} to 8 µA for 4-Mbit BL Specification change: t_{WHAX} to 20 ns for 2-/4-Mbit BL Errata: 2-Mbit 56-Lead TSOP - Pin 20 incorrect bonding to GND Specification Clarification: 10% V_{PP} option for extended temperature
05/01/96	-008	This is the new Specification Update document. It contains all identified errata published prior to this date.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This is the eighth release of the 28F400BX/BL, 28F004BX/BL, 28F200BX/BL and 28F002BX/BL Specification Update. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published.

Functional descriptions for this product are found in the *4-Mbit (256K x 16, 512 x 8) Boot Block Flash Memory Family, 4-Mbit (256K x 16, 512 x 8) Low-Power Boot Block Flash Memory Family, 2-Mbit (128K x 16, 256K x 8) Boot Block Flash Memory Family,* and
2-Mbit (128K x 16, 256K x 8) Low-Power Boot Block Flash Memory Family datasheets.

Affected Documents/Related Documents

Title	Order
4-Mbit (256K x 16, 512 x 8) Boot Block Flash Memory Family Datasheet	290451
4-Mbit (256K x 16, 512 x 8) Low-Power Boot Block Flash Memory Family Datasheet	290450
2-Mbit (128K x 16, 256K x 8) Boot Block Flash Memory Family Datasheet	290448
2-Mbit (128K x 16, 256K x 8) Low-Power Boot Block Flash Memory Family Datasheet	290449

Nomenclature

Errata are design defects or errors. These may cause the 28F400BX/BL, 28F004BX/BL, 28F200BX/BL and 28F002BX/BLs' behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation.

Documentation Changes include typos, errors, or omissions from the current published specifications.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the product's user documentation (datasheets, manuals, etc.).

SUMMARY TABLES OF CHANGES

The following tables indicate the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to in the *4-Mbit (256K x 16, 512 x 8) Boot Block Flash Memory Family, 4-Mbit (256K x 16, 512 x 8) Low-Power Boot Block Flash Memory Family, 2-Mbit (128K x 16, 256K x 8) Boot Block Flash Memory Family,* and *2-Mbit (128K x 16, 256K x 8) Low-Power Boot Block Flash Memory Family* datasheets. Intel may fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Steps

X: Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.

(No mark)
or (Blank box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page): Page location of item in this document.

Status

Doc: Document change or update will be implemented.
Fix: This erratum is intended to be fixed in a future step of the component.
Fixed: This erratum has been previously fixed.
NoFix: There are no plans to fix this erratum.
Eval: Plans to fix this erratum are under evaluation.

Row

| Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Number	Steppings			Page	Status	Errata
	A0#	A1#	A2#			
9600001	X	X	X	7	Fixed	Write State Machine Erratum (Involving Erase Suspend Mode)
9600002	X	X	X	13	Fixed	44-L PSOP Pin #3 Bonding Error
9600003	X	X	X	14	Fixed	3.3V V_{CC} Operating Range
9600004	X	X	X	14	Fixed	56-L TSOP Pin #20 Bonding Error

Specification Changes

Number	Steppings			Page	Status	Specification Changes
	A0#	A1#	A2#			
001	X	X	X	16	Doc	Program/Erase Lockout Voltage
002	X	X	X	18	NoFix	Write Timing
003	X	X	X	19	NoFix	Extended Temperature Deep Power-Down Current
004	X	X	X	20	NoFix	Commercial Temperature Deep Power-Down Current
005	X	X	X	20	NoFix	Address Hold from WE# High

Specification Clarifications

Number	Steppings			Page	Status	Specification Clarifications
	A0#	A1#	A2#			
001	X	X	X	21	NoFix	Clarification of Mirror Die Devices
002	X	X	X	22	NoFix	Clarification of 10% V_{PP} for Extended Temperature

Documentation Changes

Number	Document Revision	Page	Status	Documentation Changes
				None in this Specification Update revision

IDENTIFICATION INFORMATION

Markings

Stepping	Identifier
	Please see individual errata for product-specific mark identification

ERRATA

9600001. Write State Machine Erratum (Involving Erase Suspend Mode)

PROBLEM: The 28F400/004/200/002BX/BL enter erase suspend mode when the Erase Suspend command is written to it (while the internal Write State Machine is executing an internal erase algorithm). Polling the Status Register and RY/BY# output will signal to the system that Erase Suspend has occurred. The device is now in erase suspend to status mode and writing the Read Array command will, **in most instances**, signal the device to output array data when read. The device enters a mode referred to as "erase suspend to array." This allows system software to execute code or read data from blocks of the device.

Affected components in erase suspend to array mode will occasionally, after the Read Array command is written to them, output invalid array data due to an error in the State Machine circuitry. The device in this instance enters an invalid erase suspend mode and outputs invalid data bytes. Statistically, this has occurred approximately once every 500 erase suspend attempts.

It is important to note that even if the device is in an invalid erase suspend mode, writing the Read Status Register command will still enable transition to erase suspend to status mode and subsequent reading of Status Register data correctly. This erratum only affects array read attempts while erase is suspended.

IMPLICATION: Systems that use the 28F400/004/200/002BX/BL erase suspend feature to read the array are impacted.

WORKAROUND: The following procedure will reliably and consistently alert system software that the devices listed above have entered the invalid erase suspend mode. In almost all cases, this solution will also enable successful erase suspend. Reference the flowchart, *Erratum Identification/Resolution*, which follows, for a graphical description of the steps outlined:

Process:

I. Write the Erase Suspend command to the device.

II. Poll the Status Register to determine when Erase Suspend has been achieved.

III. Write the Read Array command to the device.

IV. Read three words/bytes of data from a block **other than that being erased**.

A. At least one of the three words/bytes should have a **known different value** compared to the other two. You must know that at least one of these words/bytes are different from the other two before writing the Erase Suspend command to the device. This can be determined by reading the device in normal read array mode.

B. Hold device addresses A_0–A_1 and A_{10}—Highest-Order-Address constant through the three reads.

C. Note: Highest-Order-Address =

A_{18} for 28F400BX, 28F400BX-L;

A_{17} for 28F004BX, 28F004BX-L,

28F200BX, 28F200BX-L;

A_{16} for 28F002BX, 28F002BX-L.

D. Toggle addresses A_2–A_9 to access different word/byte locations for the three reads.

V. If the values at these three locations **do not** match (as expected, because one of the words/bytes was determined to be different from the other two, before writing the Erase Suspend command), erase suspend to array mode has been entered successfully.

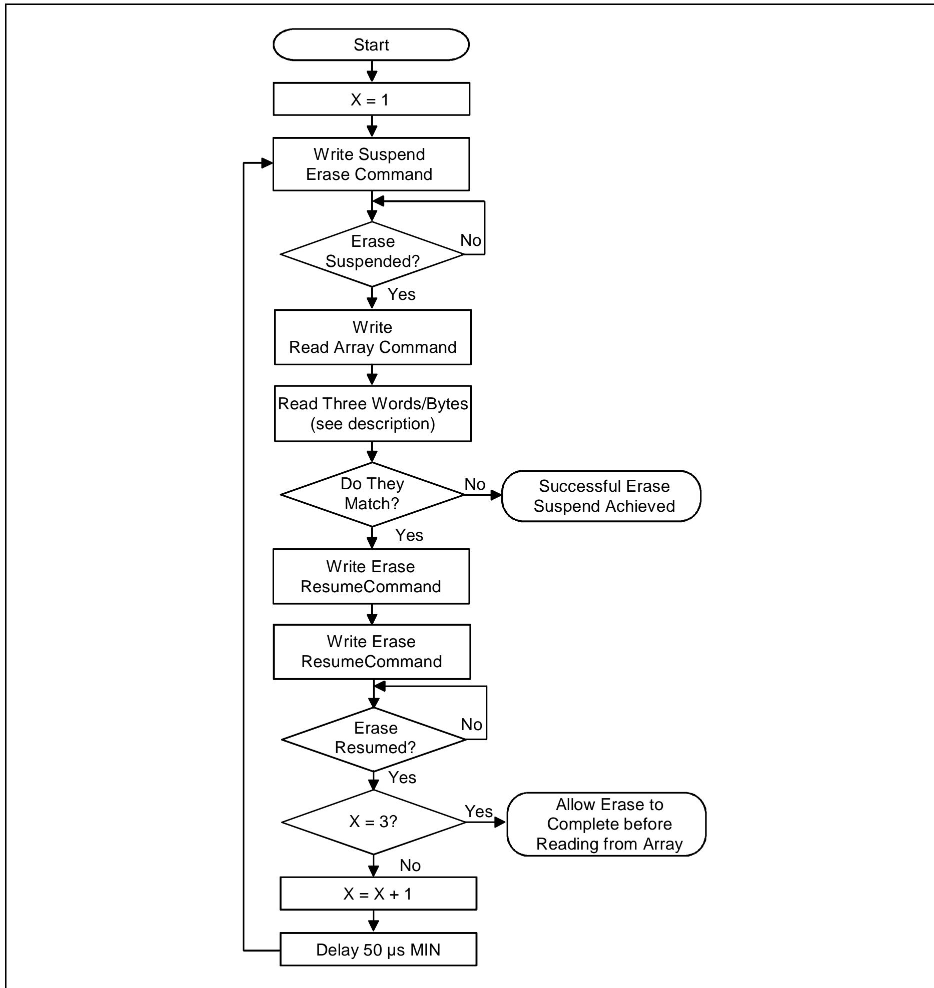
VI. If the values at these three locations match, erase suspend to array mode has not been entered successfully on this attempt. Instead, the invalid erase suspend mode has been entered. Write the Erase Resume command to the device.

VII. Read the device outputs (poll the Status Register) to determine when erase resumption has been achieved.

VIII. Wait 50 µs.

IX. Re-execute the erase suspend attempt up to two more times (or three times total).

X. If not successful after three attempts, issue the Erase Resume command, and allow the internal erase algorithm to complete before attempting to read from the array.



Erratum Identification/Resolution

Alternate Erratum Identification/Resolution

The following procedure will also reliably and consistently alert system software that the devices listed have entered the invalid erase suspend mode. This procedure should be used if the words/bytes on the component within a 256 word/byte "window" defined by A_2–A_9, are unknown. This approach is easier to implement, but may cancel erase suspends that have correctly executed, since it examines non-defined data. Nonetheless, invalid Erase Suspends will be reliably and consistently identified with this procedure. Reference the flowchart, *Alternate Erratum Identification/Resolution*, which follows, for a graphical description of the steps outlined below:

Process:

I. Write the Erase Suspend command to the device.

II. Poll the Status Register to determine when Erase Suspend has been achieved.

III. Write the Read Array command to the device.

IV. Read six words/bytes of data from a block other than that being erased.

  A. Hold device addresses A_0–A_1 and A_{10}—Highest-Order-Address constant through the six reads.

  B. Note: Highest-Order-Address =

  A_{18} for 28F400BX, 28F400BX-L;

  A_{17} for 28F004BX, 28F004BX-L,

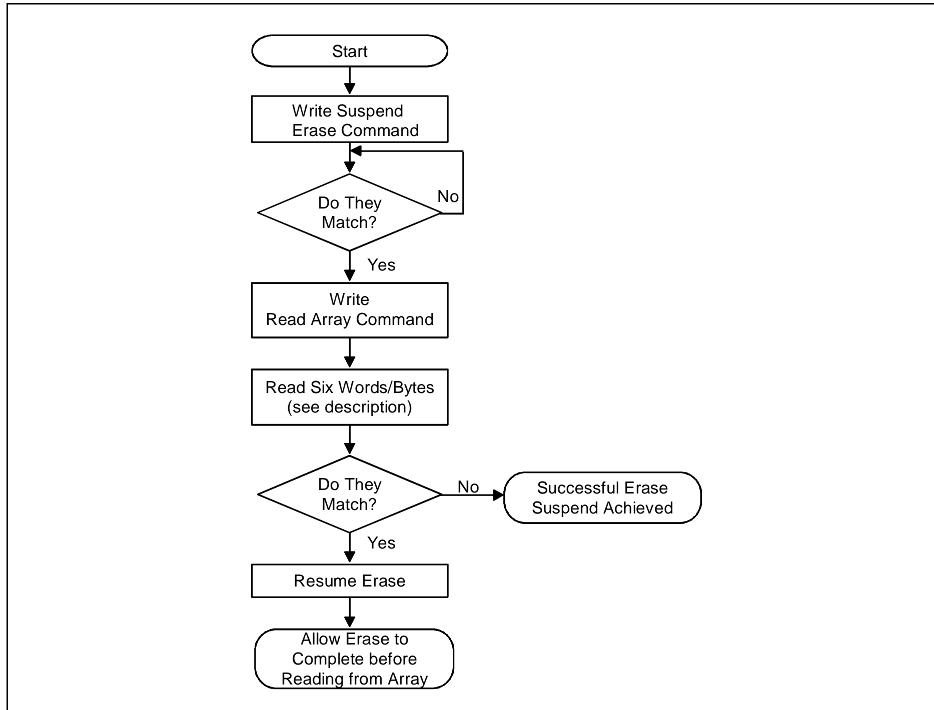
  28F200BX, 28F200BX-L;

  A_{16} for 28F002BX, 28F002BX-L.

  C. Toggle addresses A_2–A_9 to access different word/byte locations for the six reads.

V. If the values at these six locations **do not** match, erase suspend to array mode has been entered successfully.

VI. If the values at these six locations match, write the Erase Resume command to the device, read the device outputs (poll the Status Register) to determine when erase resumption has been achieved, and allow the internal erase algorithm to complete before attempting to read from the array.



Alternate Erratum Identification/Resolution

STATUS: All post-1993 materials have been fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: The 28F400BX, 28F400BL, 28F004BX, 28F004BL, 28F200BX, 28F200BL, 28F002BX and 28F002BL are affected.

Updated material will be distinguished by an indicator in the FPO field (third line) on the top-side package mark. All materials not so distinguished are affected by this erratum. Production materials which met all published datasheet specifications were available effective the first half of 1993.

This erratum only affects device operation in erase suspend mode. Customers not using erase suspend mode will not be impacted. Please see the device datasheets for a description of erase suspend mode.

9600002. 44-Lead PSOP Pin #3 Bonding Error

PROBLEM: Pin #3, which is defined as a NC (No Connect) in Intel's Flash memory datasheets, is instead shorted to ground on the affected material.

This erratum may create a problem in systems that connect an address line to pin #3 (NC) for future upgrade to Intel's 4-Mbit Boot Block flash memories. These systems will experience an electrical short between the address line and ground through pin #3 on the flash memory.

The Bond Out diagram has subsequently been corrected and all devices that are not identified as affected material (described above) will not experience a short. Pin 3 on unaffected devices will be a true NC, with nothing internally connected to this pin.

IMPLICATION: This misbonding does not cause any problems with the component itself but it does pose a problem with the next higher density (by shorting the highest order address pin to ground).

WORKAROUND: All suspected material should be replaced if a future upgrade is planned or anticipated.

STATUS: Corrected materials have been shipping since October 24, 1993. Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: The 28F200BX and 28F200BL (PSOP ONLY) are affected.

Affected material is distinguished by the first and second lines on the **bottom side** of the package. All materials that are affected can be identified by the following:

1. The first line must start with a "N."
2. The second line's last two digits must be a number less than "43."

All other materials are not affected by this erratum. This includes previously manufactured material out of D2, and all material manufactured after October 24, 1993, out of all fabrication facilities.

Example #1: Material affected by the erratum:

N31529200A	First line starts with "**N**"
200**30**	Second line's last two digits are less than **43**

Example #2: Material **not** affected by the erratum:

N31529200A	First line starts with "**N**"
200**45**	Second line's last two digits are greater than **43**

Example #3: Material **not** affected by the erratum:

221794100A	First line starts with "2," not "**N**"
200**XX**	Second line's last two digits are a don't care, since first line starts with "2"

9600003. 3.3V V_{CC} Operating Range

PROBLEM: This erratum affects the V_{CC} supply voltage tolerance specifications for the 3.3V products listed above. The currently specified tolerance for V_{CC} is 3.0V to 3.6V for read, program, and erase modes. For the affected material, this specification has changed to 3.15V to 3.6V for the program and erase modes, while the read mode V_{CC} tolerance remains 3.0V to 3.6V. All other DC and AC specifications remain unchanged. The system voltage regulation should be evaluated to ensure that these changes do not affect system operation.

The following table describes the changes to the V_{CC} supply voltage tolerance:

New V_{CC} Supply Voltage Tolerances

Symbol	Parameter	Mode	Min	Max	Unit
V_{CC}	V_{CC} Supply Voltage	Program/Erase	3.15	3.6	V
		Read	3.0	3.6	V

IMPLICATION: This erratum will be of concern to customers who have tight or no tolerance to the 3V ± 10% spec for program/erase operations. If there will be no suspending to erase, this errata should be disregarded. All suspected applications should be verified for potential data corruption.

WORKAROUND: SmartVoltage devices can be used for those applications that have issues with the new voltage limits for program/erase operations.

STATUS: All materials shipped after August, 1994, have been corrected. Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: The 28F400BL, 28F004BL are affected.

9600004. 56-Lead TSOP Pin #20 Bonding Error

PROBLEM: Pin #20, which is defined as a NC (No Connect) in Intel's Flash memory datasheets, is instead shorted to ground on the affected material.

This misbonding will create a problem in systems that connect an address line to pin #20 (NC) for future upgrade to Intel's 4-Mbit Boot Block flash memories. These systems will experience an electrical short between the address line and ground through pin #20 on the flash memory.

The Bond Out diagram has subsequently been corrected and a standard test has been implemented to verify NC connections. All devices that are not identified as affected material (described below) will not experience a short. Pin #20 on unaffected devices will be a true NC, with nothing internally connected to this pin.

IMPLICATION: The misbonding does not cause any problems with the component itself but it does pose a problem if a higher density device is placed in the same application (the misbonding effectively shorts the address input to ground).The new bond diagrams have been checked and correlated. All materials shipped since December, 1994, are properly bonded.

WORKAROUND: All suspected material should be replaced if a future upgrade is planned or anticipated.

STATUS: All materials shipped after December 8, 1994, have been corrected. Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: The 28F200BX and 28F200BL (56-Lead TSOP **only**) are affected.

Affected material is distinguished by the first line on the **top side** of the package. All material that is affected is packaged in the **56-lead TSOP** package and can be identified by the following:

1. The first line must start with a "U"
2. The second digit is "3" or "4"
3. If the second digit is "3," the next two digits must be between "38" and "52"
4. If the second digit is "4," the next two digits must be between "01" and "49"

All other materials are not affected by this erratum. This includes all material manufactured after December 8, 1994, out of all fabrication facilities.

Example #1 - Material **affected** by the erratum:

U34020P2 → First line starts with "U"
340020P2 → Second digit is "3"
3**40**020P2 → Next two digits are between "38" and "52"

Example #2 - Material **not affected** by the erratum:

U31516P4 → First line starts with "U"
31516P4 → Next digit is "3"
31516P4 → Next two digits are **before** "38"

Example #3 - Material **not affected** by the erratum:

U50137P3 → First line starts with "U"
50137P3 → Next digit is "**5**"

SPECIFICATION CHANGES

001. Program/Erase Lock-Out Voltage

PROBLEM: The devices listed above do not meet the V_{LKO}, V_{CC} Erase/Write Lock Voltage, minimum specification of 2.0 volts when operating in **3.3V** mode. Instead, the described devices meet a minimum V_{LKO} voltage of **1.7 volts**.

The V_{LKO} specification defines the V_{CC} supply voltage below which the flash memory will not accept command writes to its Command User Interface (CUI). The CUI determines the state of the flash memory, via command writes from the user. The V_{LKO} specification defines one level of protection from spurious command writes to the CUI during V_{CC} power transitions. Spurious command writes may place the flash memory in an undesired mode of operation or alter the contents of the device.

The lowered V_{LKO} specification reduces spurious-write protection using V_{LKO} at 3.3V. However, V_{LKO} is only one of several methods available for preventing unwanted command writes.

This is a permanent change and will affect all production units manufactured throughout the lifetime of these products.

WORKAROUND: ***Protection against Spurious Command Writes***

Intel Flash memories offer multiple protection mechanisms against spurious command writes, especially during power transitions. Upon power-up, the described devices are indifferent as to which supply, V_{PP} or V_{CC}, ramps first. Power supply sequencing is not required. The V_{LKO} protection mechanism inhibits command writes to the flash for V_{CC} below V_{LKO}. Additional protection methods should be used, as described below, to prevent spurious command writes for V_{CC} voltages above V_{LKO}.

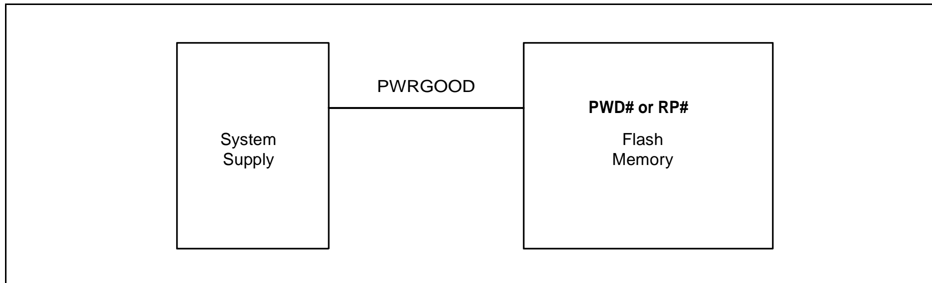
Intel Flash memories feature two-line write control, using the CE# and WE# pins. Refer to the appropriate datasheet for a complete description of commands and timings for write operations. Since both WE# and CE# must be low (active) for a command write, driving either signal to V_{IH} will inhibit command writes.

The CUI adds another level of protection by requiring a two-step command sequence before program or erase operations are executed. This requirement reduces the likelihood of a spurious command write that may affect the contents of the memory array.

To provide total protection from spurious writes, however, Intel recommends using the deep power-down/reset pin, RP#, to disable the flash memory during V_{CC} power transitions or reset operations.

Using RP# for Protection against Spurious Command Writes

To implement RP# write protection, RP# should be connected as shown in the figure below. The powergood (PWRGOOD) signal, available on most system supplies, goes low (active) when V_{CC} is removed from the system. When this occurs, RP# is forced low, the flash state machine is reset and the flash enters deep power-down mode where the flash is disabled regardless of the state of the other control pins. Upon V_{CC} power-up the power-good signal, and hence RP#, is forced high and the flash transitions to read array mode.



Using RP# for Protection against Spurious Command Writes

The RP# high to valid output delay, t_{PHQV}, is optimized to work with a host of high-performance CPUs, ensuring that the flash memory transitions to the read array mode before a read is attempted by the system CPU. Discrete low-V_{CC} detect components that generate PWRGOOD are available from Maxim and Motorola, as well as other vendors.

Refer to the datasheets for a complete description of RP# usage. Figure 1 in each datasheet shows a typical system interface to flash including RP# interface.

AFFECTED PRODUCTS: The 28F400BL, 28F004BL, 28F200BL and 28F002BL are affected.

002. Write Timing

PROBLEM: This change affects two write timing specifications for the –80 ns products listed above. The minimum “pulse width low” (t_{CPL}) specification increases from 50 ns to 60 ns on affected material for both CE#-controlled writes and WE#-controlled writes. The minimum “pulse width high” (t_{CPH}) specification decreases from 30 ns to 20 ns for both CE#-controlled writes and WE#-controlled writes. Total “write cycle time” (t_{WC}) remains unchanged. System write timing should be evaluated to ensure these changes do not affect system operation.

If it is determined that these changes cause system timing problems, the –60 ns products can be used, as these products are unaffected by this change.

The following tables describe the changes to the write timing specifications. Please refer the *4-Mbit (256K x 16, 512 x 8) Boot Block Flash Memory Family, 4-Mbit (256K x 16, 512 x 8) Low-Power Boot Block Flash Memory Family, 2-Mbit (128K x 16, 256K x 8) Boot Block Flash Memory Family,* and *2-Mbit (128K x 16, 256K x 8) Low-Power Boot Block Flash Memory Family* datasheets for timing waveforms for these specifications.

WE#-Write Timing Specifications Changes for –80 ns Products

Specification		Description	Unaffected Material	Affected Material	Comment
t_{AVAV}	t_{WC}	Write Cycle Time	80 ns	80 ns	Unchanged
t_{WLWH}	t_{WP}	WE# Pulse Width	50 ns	60 ns	Increases 10 ns
t_{WHWL}	t_{WPH}	WE# Pulse Width High	30 ns	20 ns	Decreases 10 ns

CE#-Write Timing Specifications for –80 ns Products

Specification		Description	Unaffected Material	Affected Material	Comment
t_{AVAV}	t_{WC}	Write Cycle Time	80 ns	80 ns	Unchanged
t_{ELEH}	t_{CP}	CE# Pulse Width	50 ns	60 ns	Increases 10 ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	30 ns	20 ns	Decreases 10 ns

AFFECTED PRODUCTS: The 28F400BX, 28F004BX, 28F200BX and 28F002BX are affected.

The third line of the "top-side" mark is the Finished Processing Order (FPO) number. If the FPO number has eight characters it is not affected by this change. If the FPO number has nine characters **and** is a –80 part (80 ns), it is affected by this change.

Example #1:
E28F004
BX-T80 → **–80** part, look at FPO number
T32200F9 → FPO number with 8 characters, therefore **not affected**
m c 1992

Example #2:
E28F004
BX-T80 → **–80** part, look at FPO number
T32200F9P→ FPO number with 9 characters, therefore **affected**
m c 1992

Example #3:
E28F004
BX-T60 → **Not –80** part, therefore **not affected**
T32200F9P→ FPO number with 9 characters, but **not affected**
m c 1992

003. Extended Temperature Deep Power-Down Current

PROBLEM: This change affects the I_{CCD} max deep power-down current specifications for the products listed above **during extended temperature operation only**. The I_{CCD} max. specification increases from 8 µA to 20 µA on affected material for extended temperature operation.

The following table describes the changes to the I_{CCD} specifications:

New I_{CCD} Deep Power-Down Current Specifications

Symbol	Parameter	Typ	Max	Unit	Test Conditions
I_{CCD}	V_{CC} Deep Power-Down Current	0.20	20	µA	RP# = GND ± 0.2V

AFFECTED PRODUCTS: The 28F400BX, 28F004BX, 28F200BX and 28F002BX are affected.

004. Commercial Temperature Deep Power-Down Current

PROBLEM: This change affects the I_{CCD} max deep power-down current specifications for the products listed above **during commercial temperature operation only**. The I_{CCD} max. specification increases from 1.2 µA to 8 µA on affected material for commercial temperature operation.

The following table describes the changes to the I_{CCD} specifications:

New I_{CCD} Deep Power-Down Current Specifications

Symbol	Parameter	Typ	Max	Unit	Test Conditions
I_{CCD}	V_{CC} Deep Power-Down Current	0.12	8.0	µA	RP# = GND ± 0.2V

AFFECTED PRODUCTS: The 28F400BX, 28F004BX, 28F200BX and 28F002BX are affected.

005. Address Hold from WE# High

PROBLEM: This change affects the t_{WHAX} timing specification for the products listed above. The t_{WHAX} max. specification increases from 10 ns to 20 ns on affected material at **3.3V operation**.

The following table describes the changes to the t_{WHAX} specifications:

New t_{WHAX} Timing Specification

Symbol	Parameter	Typ	Max	Unit	Test Conditions
t_{WHAX}	Address hold from WE# high	10	20	ns	

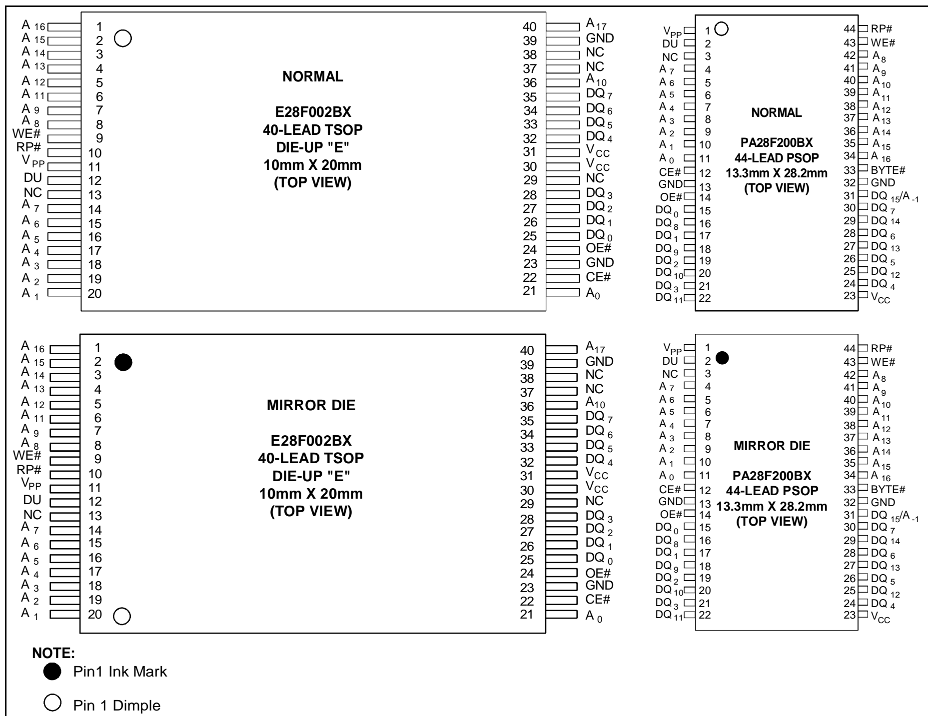
AFFECTED PRODUCTS: The 28F400BL, 28F004BL, 28F200BL and 28F002BL are affected.

SPECIFICATION CLARIFICATIONS

001. Clarification of Mirror Die Devices

PROBLEM: The die from the first few lots of the 28F200/002BX 2-Mbit Boot Block flash memory were mirror-imaged. These mirrored die have been qualified and found to be identical in every way to subsequent normal devices. However, some package markings had to be altered to identify this difference.

The 28F200/002BX is offered in the die-up TSOP and PSOP packages. Affected materials include both the 40-lead TSOP and the 44-lead PSOP packages. After some testing and package assessment, the mirrored die was inversely placed (i.e., built as die-down) in the die-up packages. A white dot is painted on the top, near the left-hand corner to indicate the position of pin 1. The distinguishing characteristics of these different package types are explained in the *Pin Identification* figure below.



Pin Identification

AFFECTED PRODUCTS: The 28F200BX and 28F002BX are affected.

Affected materials will be distinguished by an ink **mark** indicator for pin 1 in the upper left-hand corner of the device. All material not affected by this erratum will have the normal pin 1 dimple in the upper left hand corner. If the ink mark is present, the dimple should be ignored. There are some devices on which the ink mark indicating pin 1 is absent. If a device is suspected to be a mirrored-die product, please contact the local Intel representative for a replacement.

This erratum does not affect the functionality of these devices in any way. Although the die orientation is reversed, the device functions as a normal 28F200/002BX device because the internal circuitry of these die is the mirror-image of the normal die. All specifications and documentation available for the normal devices is also valid for the mirrored-die products. The packages affected are the 40-lead TSOP and 44-lead PSOP.

002. Clarification of 10% V_{PP} for Extended Temperature

PROBLEM: The datasheet provides a 10% V_{PP} options when using the standard 28F400/004BX-T/B and 28F200/002BX-T/B. At the commercial temperature range, a table specifies program and erase times at 5% and 10% V_{PP}. For extended temperatures, there is only a table specifying 5% V_{PP} tolerance. This is because these **devices do not support the 10% V_{PP} option at extended temperatures**. The datasheet is correct as is.

AFFECTED PRODUCTS: The 28F400BX, 28F004BX, 28F200BX and 28F002BX are affected.

DOCUMENTATION CHANGES

There are no documentation changes in this Specification Update revision.