# 28F008SA/SA-L
# SPECIFICATION UPDATE

Release Date: February 1997

Order Number 297183-007

The 28F008SA/SA-L may contain design defects or errors known as errata. Characterized errata that may cause the 28F008SA/SA-Ls' behavior to deviate from published specifications are documented in this specification update.

Intel Corporation
P.O. Box 7641
Mt. Prospect, IL 60056-7641

or call in North America 1-800-879-4683, Europe 44-0-1793-431-155, France 44-0-1793-421-777,

Germany 44-0-1793-421-333 other Countries 708-296-9333

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# REVISION HISTORY

| Date of Revision | Version | Description |
|---|---|---|
| 04/07/94 | -001 | Document includes all known errata to date: erase suspend flowchart, Write State Machine, $I_{CCD}$ deep power-down current. |
| 05/31/94 | -002 | File dates linked to system clock corrected. |
| 07/29/94 | -003 | Identification information added to Write State Machine erratum. |
| 08/24/94 | -004 | Added extended temperature addendum. |
| 06/22/95 | -005 | Corrected device identification for 28F008SA-L<br>28F008SA-L150 Commercial Specifications<br>Added GSM phone specifications. |
| 05/01/96 | -006 | This document has been converted to the new Specification Update format. It contains all identified errata published prior to this date.<br>Added reset specifications<br>Removed 28F008SA-L150, GSM, and extended temperature specifications<br>Revised deep power-down erratum. |
| 02/01/97 | -007 | Removed erase suspend flowchart document change. This change was integrated into datasheet revision -002.<br>Added $V_{PP}$ Standby Current Erratum. |

## PREFACE

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This is the seventh release of the 28F0008SA/SA-L Specification Update. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published.

Functional descriptions for this product are found in the *28F008SA 8-Mbit (1 Mbit x 8) FlashFile™ Memory* and *28F008SA-L 8-Mbit (1 Mbit x 8) FlashFile™ Memory* datasheets.

### *Affected Documents/Related Documents*

| Title | Order |
|---|---|
| *28F008SA 8-Mbit (1 Mbit x 8) FlashFile™ Memory Datasheet* | 290429 |
| *28F008SA-L 8-Mbit (1 Mbit x 8) FlashFile™ Memory Datasheet* | 290435 |

### *Nomenclature*

**Errata** are design defects or errors. These may cause the 28F0008SA/SA-Ls' behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

**Specification Changes** are modifications to the current published specifications.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation.

**Documentation Changes** include typos, errors, or omissions from the current published specifications.

**NOTE:**

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

## SUMMARY TABLES OF CHANGES

The following tables indicate the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to *28F008SA 8-Mbit (1 Mbit x 8) FlashFile™ Memory* and *28F008SA-L 8-Mbit (1 Mbit x 8) FlashFile™ Memory* datasheets. Intel may fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

### *Codes Used in Summary Tables*

#### *Steps*

| | |
|---|---|
| X: | Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping. |
| (No mark) or (Blank box): | This erratum is fixed in listed stepping or specification change does not apply to listed stepping. |

#### *Page*

| | |
|---|---|
| (Page): | Page location of item in this document. |

#### *Status*

| | |
|---|---|
| Doc: | Document change or update will be implemented. |
| Fix: | This erratum is intended to be fixed in a future step of the component. |
| Fixed: | This erratum has been previously fixed. |
| NoFix: | There are no plans to fix this erratum. |
| Eval: | Plans to fix this erratum are under evaluation. |

#### *Row*

| | |
|---|---|
| \| | Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document. |

## Errata

| Number | Steppings | | | Page | Status | Errata |
|---|---|---|---|---|---|---|
| | A-0 | A-1 | B-0 | | | |
| 1 | X | | | 7 | Fixed | Write State Machine Erratum (Involving Erase Suspend Mode) |
| 2 | | | X | 12 | Eval | $V_{PP}$ Standby Current for the 28F008SA |

## Specification Changes

| Number | Steppings | | | Page | Status | Specification Changes |
|---|---|---|---|---|---|---|
| | A-0 | A-1 | B-0 | | | |
| 1 | | | X | 13 | Doc | $I_{CCD}$ Deep Power-Down Current for the 28F008SA |
| 2 | | | X | 13 | Doc | Reset Specifications for the 28F008SA |

## Specification Clarifications

| Number | Steppings | | | Page | Status | Specification Clarifications |
|---|---|---|---|---|---|---|
| | A-0 | A-1 | B-0 | | | |
| N/A | | | | 15 | | None in this Specification Update revision. |

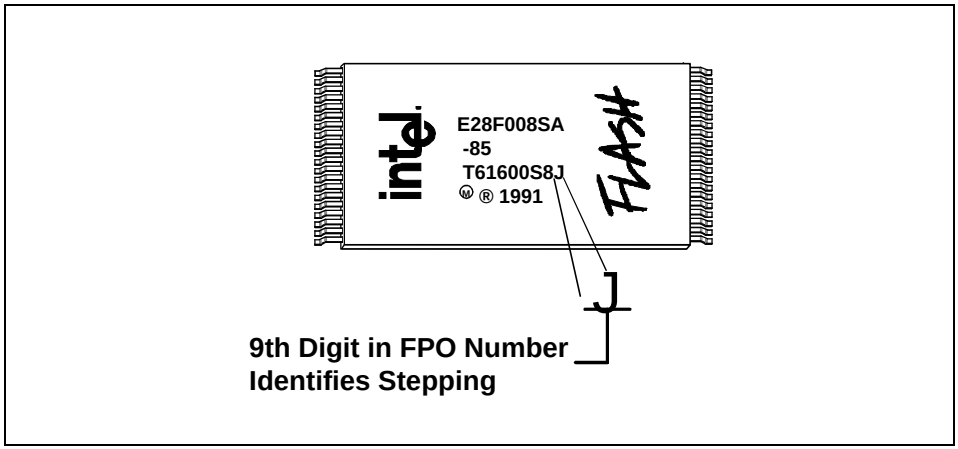
## Documentation

| Number | Document Revision | Page | Status | Documentation Changes |
|---|---|---|---|---|
| N/A | | 15 | | None in this Specification Update revision. |

## IDENTIFICATION INFORMATION

### *Markings*

The Finished Processing Order (FPO) number identifies the device stepping, as illustrated below:




**FPO Number Location and Clarification**

| Stepping | Identifier |
|---|---|
| A-0 Stepping | Ninth digit on topside FPO mark (third line) = “B” |
| A-1 Stepping | Ninth digit on topside FPO mark (third line) = “C, D, E, F, G, S, T, X, Z” |
| B-0 Stepping | Ninth digit on topside FPO mark (third line) = “U, V” |

# ERRATA

## *1. Write State Machine Erratum (Involving Erase Suspend Mode)*

**PROBLEM:** The 28F008SA and 28F008SA-L enter erase suspend mode when the Erase Suspend command is written to it (while the internal Write State Machine is executing an internal erase algorithm). Polling the Status Register and RY/BY# output will signal to the system that Erase Suspend has occurred. The device is now in erase suspend to status mode and writing the Read Array command will, **in most instances**, signal the device to output array data when read. The device enters a mode referred to as “erase suspend to array.” This allows system software to execute code or read data from blocks of the device.

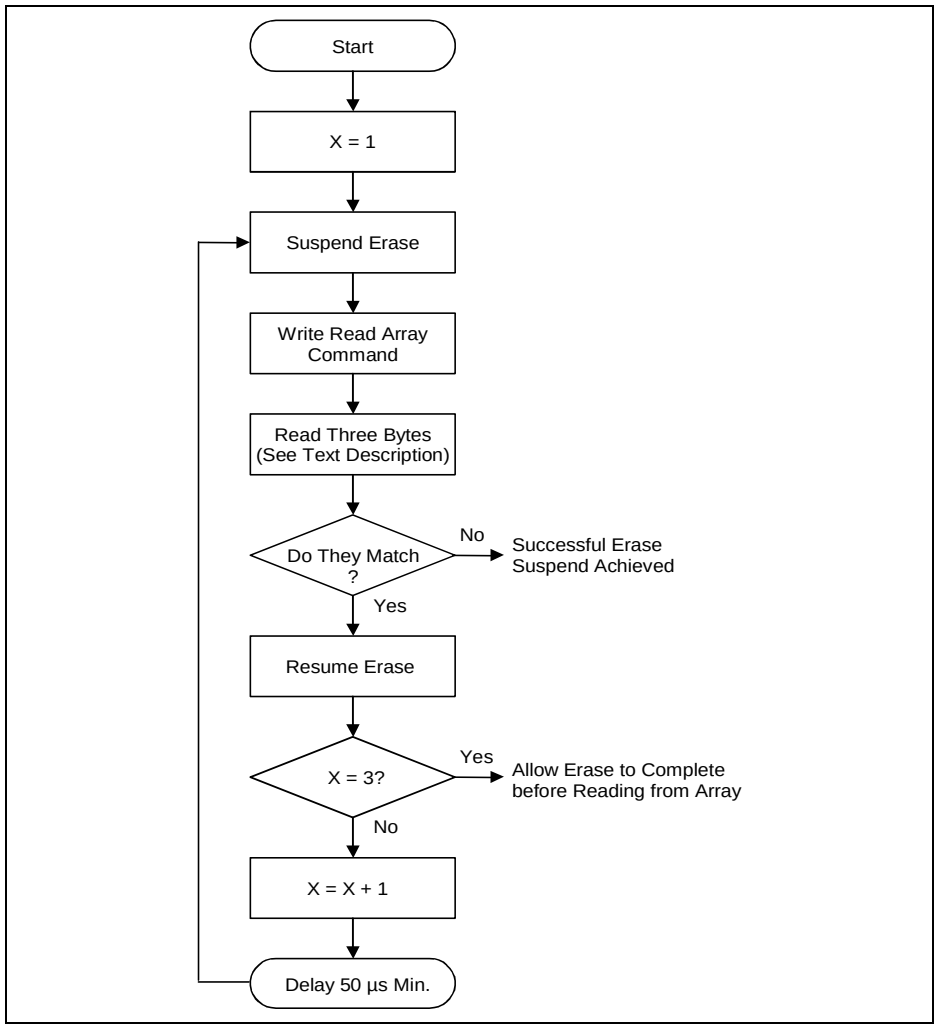
Affected components in erase suspend to array mode will occasionally, after the Read Array command is written to them, output invalid array data due to an error in the State Machine circuitry. The device in this instance enters an invalid erase suspend mode and outputs invalid data bytes. Statistically, this has occurred approximately once every 500 erase suspend attempts.

It is important to note that even if the device is in an invalid erase suspend mode, writing the Read Status Register command will still enable transition to erase suspend to status mode and subsequent reading of Status Register data correctly. This erratum only affects array read attempts while erase is suspended.

**IMPLICATION:** Systems that use the 28F008SA or 28F008SA-L erase suspend feature to read the array are impacted.

**WORKAROUND:** The following procedure will reliably and consistently alert system software that the 28F008SA/28F008SA-L has entered the invalid erase suspend mode. In almost all cases, this solution will also enable successful erase suspend. Reference the *Erratum Identification/Resolution* figure for a graphic description of the steps outlined below:

1. Write the Erase Suspend command to the device.
2. Poll the Status Register to determine when Erase Suspend has been achieved.
3. Write the Read Array Command to the device.
4. Read three bytes of data from a block **other than that being erased**.
   - At least one of the three bytes should have a **known different value** compared to the other two.
   - Hold device addresses $A_0$–$A_1$ and $A_{10}$–$A_{19}$ constant through the three reads.
   - Toggle addresses $A_2$–$A_9$ to access different byte locations for the three reads.
5. **If the values at these three locations DO NOT match (as expected), you have successfully entered erase suspend to array mode.**
6. If the values at these three locations match, you have not successfully entered erase suspend to array mode on this attempt. Instead, you have entered the invalid erase suspend mode.
   - Write the Erase Resume command to the device.
7. Read the device outputs (poll the Status Register) to determine when erase resumption has been achieved.
8. Wait 50 µs.
9. Re-execute the erase suspend attempt up to two more times (or three times total).
10. If not successful after three attempts, issue the Erase Resume command, and allow the internal erase algorithm to complete before attempting to read from the array.

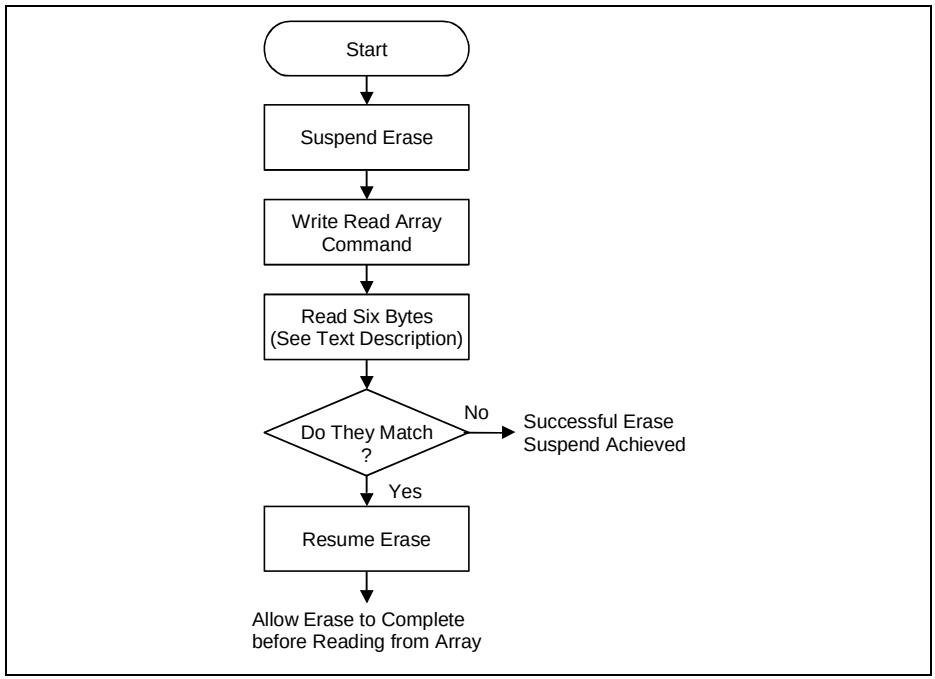



**Erratum Identification/Resolution**

**Alternate Identification/Resolution**

The following procedure will also reliably and consistently alert system software that the 28F008SA/28F008SA-L has entered the invalid erase suspend mode. This procedure should be used if the system cannot identify unique bytes on the component within a 256-byte "window" defined by $A_2$–$A_9$. This approach is easier to implement, but may cancel erase suspends that have correctly executed, since it examines undefined data. Reference the *Alternate Identification/Resolution* figure, which follows, for a graphic description of the steps outlined below:

1. Write the Erase Suspend command to the device.
2. Poll the Status Register to determine when Erase Suspend has been achieved.
3. Write the Read Array Command to the device.
4. Read six bytes of data from a block **other than that being erased**.
   - Hold device addresses $A_0$–$A_1$ and $A_{10}$–$A_{19}$ constant through the six reads.
   - Toggle addresses $A_2$–$A_9$ to access different byte locations for the six reads.
5. **If the values at these six locations DO NOT match, you have successfully entered erase suspend to array mode.**
6. If the values at these six locations match, write the Erase Resume command to the device, read the device outputs (poll the Status Register) to determine when erase resumption has been achieved, and allow the internal erase algorithm to complete before attempting to read from the array.




**Alternate Identification/Resolution**

**STATUS:** This erratum has been fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

**AFFECTED PRODUCTS:** A-0 stepping material is affected.

## 2. $V_{PP}$ Standby Current for the 28F008SA

**PROBLEM:** With $V_{PP}$ at GND, $I_{PPS}$ deviates from the published value. This deviation only affects the negative current value listed in the datasheet. The positive current specification, +15 µA, remains valid.

| Sym | Parameter | Notes | 5.0V $V_{CC}$ | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | Typ | Max | | |
| $I_{PPS}$ | $V_{PP}$ Standby Current | 1 | | +15/ -300 | µA | $V_{PP}$ = GND |

**NOTE:**

1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (packages and speeds).

If $V_{PP}$ is greater than or equal to $V_{CC}$, $I_{PPS}$ adheres to the datasheet specification of ±15 µA.

**IMPLICATION:** This erratum only affects systems that switch $V_{PP}$ to GND.

**WORKAROUND:** None.

**STATUS:** Plans to fix this erratum are under evaluation. Refer to Summary Table of Contents to determine the affected stepping.

**AFFECTED PRODUCTS:** B-0 stepping is affected by this erratum.

# SPECIFICATION CHANGES

## 1. $I_{CCD}$ Deep Power-Down Current for the 28F008SA

**PROBLEM:** $I_{CCD}$ deviates from the published to *28F008SA 8-Mbit (1 Mbit x 8) FlashFile™ Memory Datasheet* specifications. Please replace the existing datasheet $I_{CCD}$ entry with the following information. This specification change will be integrated into the next datasheet revision.

| Symbol | Parameter | Notes | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $I_{CCD}$ | $V_{CC}$ Deep Power-Down Current | 1 | | | 16(2) | µA | RP# = GND ± 0.2V<br>$I_{OUT}$ (RY/BY#) = 0 mA |

**NOTES:**
1. All currents are in RMS unless otherwise noted. Typical values at $V_{CC}$ = 5.0V, $V_{PP}$ =12.0V, T = +25°C, These currents are valid for all product versions (packages and speeds).
2. For devices with a "D" in these 8th digit of the FPO number, $I_{CCD}$ equals 60 µA.

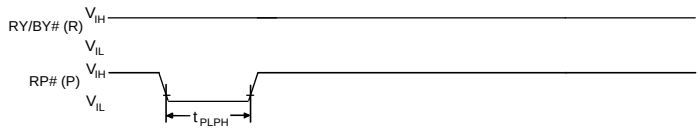
Please note that these revisions only affect current consumption in deep power-down mode. All other functions of the RP# pin are preserved. These include:

- Write protection during system power transitions
- Termination of device automation upon deep power-down mode entry
- Device reset to read array mode upon exit from deep power-down

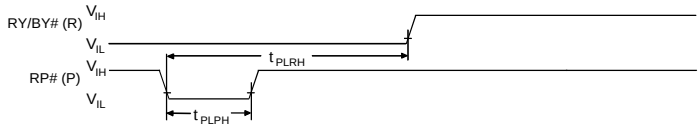
**AFFECTED PRODUCTS:** All B-0 stepping material is affected.

## 2. Reset Specifications for the 28F008SA

**PROBLEM:** Two reset specifications have been added to the 28F008SA. Please add this information the existing datasheet. The next datasheet revision will incorporate these reset specifications.




**(A) Reset during Read Array Mode**




**(B) Reset during Byte Write or Block Erase**

**AC Waveform for Reset Operation**

**Reset AC Specifications(1)**

| Sym | Parameter | Notes | $V_{CC}$ = 5V | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $t_{PLPH}$ | RP# Pulse Low Time<br>(If RP# is tied to $V_{CC}$, this specification is not applicable) | | 100 | | ns |
| $t_{PLRH}$ | RP# Low to Reset during Block Erase or Byte Write<br>(If RP# is tied to $V_{CC}$, this specification is not applicable) | 2,3 | | 12 | µs |

**NOTES:**
1. These specifications are valid for all product versions (packages and speeds).
2. If RP# is asserted while a block erase or byte write operation is not executing, the reset will complete within 100 ns.
3. A reset time, $t_{PHQV}$, is required from the latter of RY/BY# or RP# going high until outputs are valid.

In read modes, RP#-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. RP# must be held low for a minimum of 100 ns. Time $t_{PHQV}$ is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase or byte write, RP#-low will abort the operation. RY/BY# remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written.

**AFFECTED PRODUCTS:** All B-0 stepping material is affected.

## SPECIFICATION CLARIFICATIONS

There are no specification clarifications in this Specification Update revision.

## DOCUMENTATION CHANGES

There are no specification clarifications in this Specification Update revision.