intel®

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APPLICATION NOTE

Designing Flexible Sockets for Intel's Boot Block Flash Memories

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REVISION HISTORY

Number	Description
-001	Original Version

1.0 INTRODUCTION

A flexible socket is one that can use devices from different manufacturers and accommodate the variations that may exist between the parts. This allows purchasing and manufacturing flexibility that can ameliorate supply fluctuations and other issues.

This application note will discuss the issues involved in designing a flexible socket which will accommodate both Intel Smart 5 boot block flash memories and similar devices from Advanced Micro Devices. Although the specific information supplied is for the Intel Smart 5 and AMD 5V-Only product lines, the general concepts can be applied to other Intel products, such as the SmartVoltage boot block, AMD LV-series, or other manufacturer's products.

1.1 What Parts Can Be Flex Socketed?

This application note deals with Intel and AMD boot block devices only. In general, each Intel boot block product has a corresponding AMD product that can be designed into a flexible socket that can accommodate both parts. The device selection depends on the desired operating voltage of the system design.

1.1.1 2.7V–3.6V DESIGNS

For low-voltage designs operating in the 2.7V–3.6V or 3.3 ± 0.3V voltage ranges, a flexible socket design should design in Intel's SmartVoltage 28Fx00CE (x8/x16) or 28F00xBE (x8) series flash devices, along with AMD's Am29LVx00 or Am29LV00x series parts. The corresponding part numbers are shown in Appendix A.

1.1.2 4.5V–5.5V DESIGNS

The 5V designs operating in the 4.5V–5.5V voltage range, a flexible socket design should design in Intel's Smart 5 boot block products, which are named 28Fx00B5 (x8/x16), along with AMD's Am29Fx00 series parts. Another option may be to use Intel's 28Fx00BV/CV or 28F00xBV SmartVoltage devices (in their 5V operating range) along with the corresponding 5V-only Am29Fx00/00x part. The corresponding part numbers are shown in Appendix A.

2.0 DESIGNING A FLEX SOCKET

The following sections present in detail the issues involved in designing a flexible socket that will accommodate both Intel and AMD boot block products. To simplify the discussion, only the Intel 28Fx00B5 and AMD 29Fx00 parts will be examined. However, all of the concepts introduced can be applied to other product combinations at other voltages.

A flexible socket design involves solving several issues. The primary difference is in the pinout, then a number of other issues must be evaluated for possible impact on a specific design and addressed if necessary. These issues include address/data latching, DC/AC specs, Intelligent ID, command sequences, block locking and main block Sizes.

2.1 Pinout Differences

The Intel 28Fx00 and AMD 29Fx00 components are available in a number of packages, but have only two in common, the 44-lead PSOP and the 48-lead TSOP. These packages have a few minor pinout differences that can be easily accommodated.

2.1.1 44-LEAD PSOP DIFFERENCES

The 44-lead PSOP pinout contains two pins that differ between the Intel 28Fx00 and AMD Am29Fx00 or 29lvx00 products. These pinouts are shown in Figure 1.

1. Intel's V_{PP} pin is NC (No Connection) on AMD. V_{PP} is the program/erase voltage supply (5V or 12V). Since it is not connected on the AMD part, running V_{PP} voltage out to that pin to support Intel program/erase should not cause any problems for the AMD device. While unnecessary, a jumper can be used to prevent power from reaching the AMD device's NC pin, if additional safety is desired.
2. Intel's WP# pin is AMD's RY/BY# pin. WP# is a logic-level input controlling lock/unlock of the boot block. AMD's RY/BY# is a output that indicates the ready/busy status of their internal state machine. This conflict needs a jumper or similar solution to solve.

Table 1. 44-Lead PSOP Pinout Differences

Pin	Intel Pin	AMD Pin	Description
1	V_{PP}	NC	Program/Erase Power
2	WP#	RY/BY#	Write Protect Input (Intel) / Ready/Busy Signal (AMD)

A jumper or switch solution is required to resolve the pinout mismatch between Intel's WP# pin and AMD's RY/BY# pin. The Intel WP# pin, being a CMOS input, cannot be floated and needs to be driven either high or low (or controlled by a signal, if locking control is needed). This pin can not be floated or improper device operation can result. The AMD RY/BY# pin is an output showing the busy status of the internal state machine. Since this feature is not supported on the Intel device, it should not be used (common denominator approach) and software polling of the status register should be used to read ready/busy status for both parts. The jumper should switch between GND/V_{CC}/Control signal (depending on the desired lock status of the boot block) when using Intel devices, and float for the AMD device (so that the AMD output is not in contention with any signals intended to drive the WP# pin).

2.1.2 48-LEAD TSOP DIFFERENCES

The 48-lead TSOP pinout contains three pins that differ between the Intel 28Fx00 and AMD Am29Fx00 products. These pinouts are shown in Figure 2.

1. Intel's V_{PP} is NC (Not Connected) on the AMD pinout. V_{PP} is the program/erase voltage supply (5V or 12V). Since it is not connected on the AMD part, running V_{PP} voltage out to that pin to support Intel program/erase should not cause any problems for the AMD device.
2. Intel's WP# pin is NC on the AMD pinout. WP# is a logic-level input controlling lock/unlock of the boot block. Since it is not connected on the AMD part, connecting this pin to V_{CC}, Ground, or a control signal to support Intel boot block locking function should not cause any problems for the AMD device.
3. AMD's RY/BY# pin is NC (Not Connected) on Intel's pinout, so there is no pin conflict, but since this feature is not supported on the Intel device, it should not be used and software polling of the status register should be used to read ready/busy status for both parts.

Table 2. 48-Lead TSOP Pinout Differences

Pin	Intel Pin	AMD Pin	Description
13	V_{PP}	NC	Program/Erase Power
14	WP#	NC	Write Protect Pin
15	NC	RY/BY#	Ready/Busy Output

All pins that differ between the components are not connected on the other device.

Intel's V_{PP} pin should be connected to a 5V or 12V supply, which should not affect the AMD device since that pin is not connected. A jumper can be used to prevent power from reaching the AMD device's NC pin, if additional safety is desired.

Intel's WP# pin has no conflict with AMD's NC pin, but, being a CMOS input, needs to be driven either high or low (or controlled by a signal, depending on the type of locking control needed). This pin can not be floated or improper device operation can result. Since Pin 14 is NC on the AMD device, these signals should have no effect on it.

Since Intel boot block devices do not have a ready/busy pin, software polling should be used to check status for both devices. Pin 15 should either be left unconnected or a jumper used to connect the RY/BY# function.

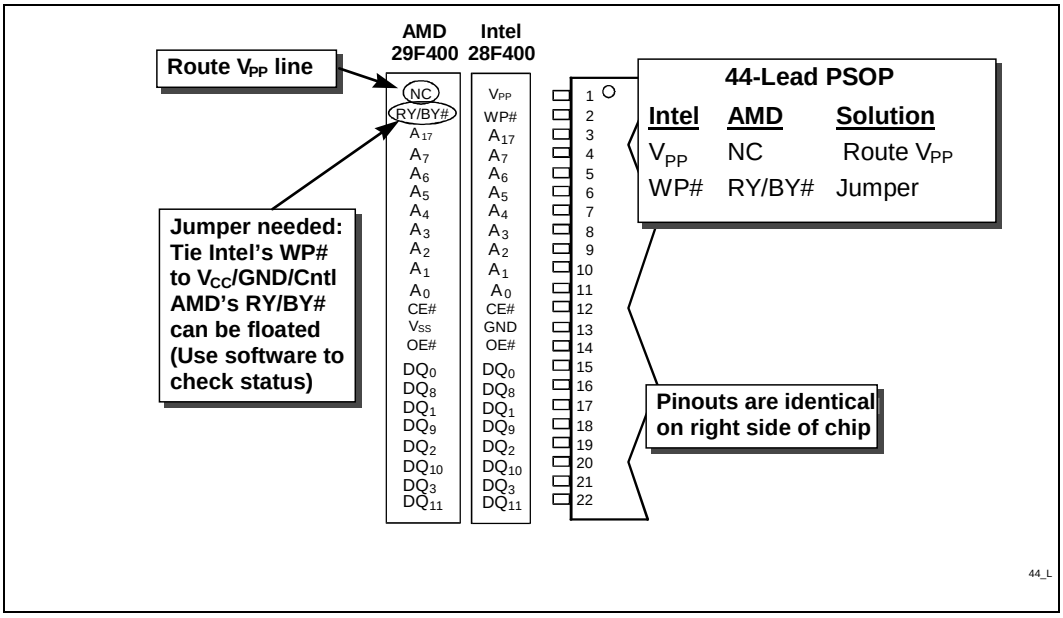

Figure 1. 44-Lead PSOP Pinout Configuration

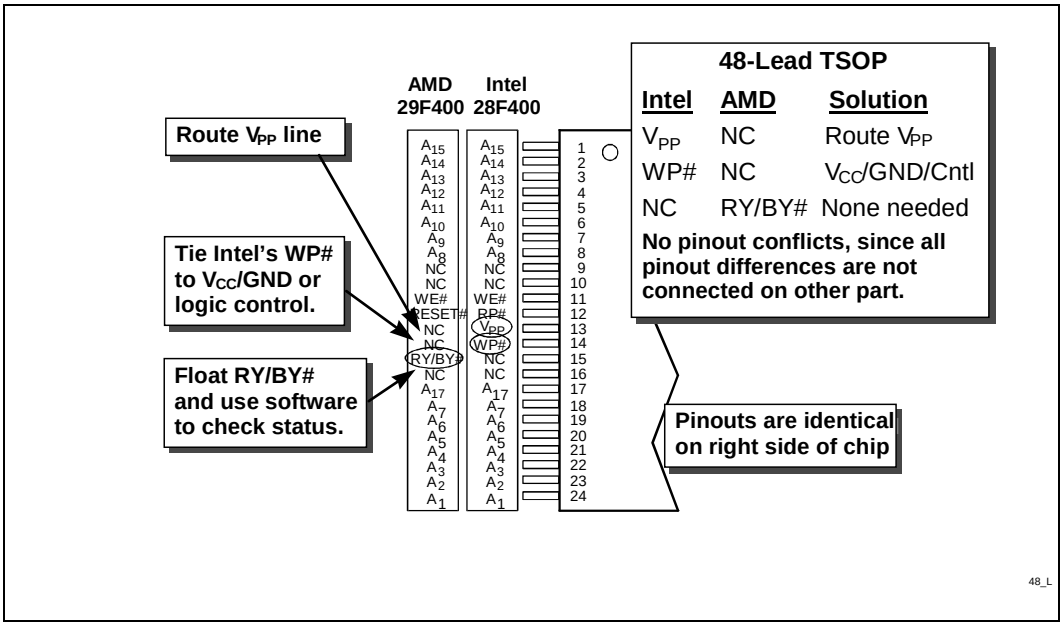

Figure 2. 48-Lead TSOP Pinout Comparison

2.2 Address/Data Latching

A key difference in the operation of Intel and AMD flash devices is the latching of addresses and data during a write cycle. As shown in Figure 3, Intel devices latch both the address and data at the same time upon the rising edge of the write signal, while AMD devices latch the address and data on separate edges, the address on the falling edge and the data on the rising edge of the write signal.

While it may be possible for the interface timings to work out such that both Intel and AMD timings are already met, every microcontroller/microprocessor has different restrictions on address/data setup and hold, so each specific combination must be evaluated.

If possible, set up the setup and hold timings such that the address and data are setup early enough and held long enough to be latched by both the rising and falling edges. This would allow Intel or AMD parts to be placed into a site and work properly without any configuration changes.

Since software control of the flash component requires proper writes to the part, this measure must be implemented before any of the software measures, such as intelligent identifier reads and command set switching, can work.

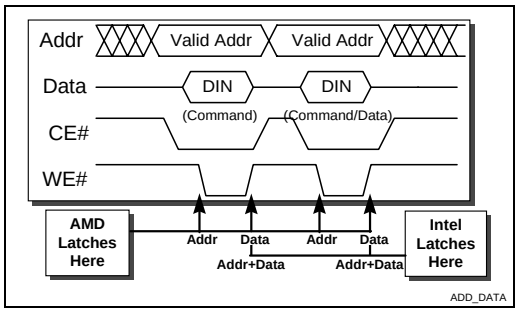

Figure 3. Differences in Address/Data Latching

2.3 DC and AC Specifications

These devices may differ in many other specification differences which system designers should account for in a dual design. Because of the large number of DC and AC specifications, they will not all be evaluated here. The datasheets should be compared during the design of a flexible socket system A few key issues to note during this comparison will be discussed in the following sections.

2.3.1 DC CHARACTERISTICS

When comparing power and current specifications, take note of the test conditions, especially the read frequency. Power/Current specs should be compared at the actual read frequency for the system, which can be calculated by inverting the read access time of the system. To equalize read frequencies between components, use the approximate rule for Intel components that I_{CC} read current is related to frequency by 4 mA/MHz, so for every increase of 1 MHz of read frequency, read current increases about 4 mA. Correspondingly, a decrease of 1 MHz in read frequency reduces read current by about 4 mA.

2.3.2 AC CHARACTERISTICS

Designers should compare timing specifications and accommodate any differences for a dual site layout. In particular, be aware of the difference in rising/falling edge latching, which is discussed in Section 2.2.

2.4 Intelligent Identifier

The intelligent identifiers are codes that can be read from an internal register in the flash. They identify the manufacturer of the device and the type of device. These codes can be read using both hardware and software methods. Intel and AMD components use the same hardware method for reading identifier information: taking A_9 to a high voltage (about 12V). Both manufacturers also provide software command sequences for reading identifier information. While these sequences are different, they are easily accommodated with a modified software routine.

Figure 4 shows an algorithm that can distinguish between Intel and AMD components, providing interface commands applicable to most AMD and Intel components. Validate these commands using the datasheets for the specific components in use. Command sequences for other flash vendors can also be substituted as appropriate. The example algorithm shown above should be able to identify between Intel and AMD flash. The basic idea is this: first read the ID (using Intel commands). If the ID is Intel, then the determination is complete: it is Intel Flash. If the ID is not Intel, then you read the ID (using AMD commands). If the ID is AMD, then the determination is complete: it is AMD flash. If not, then identification has failed. (maybe another company is in there). If other manufacturers besides AMD and Intel are to be included in the sourcing, the algorithm will need to be expanded to include those ID checks. The result of this identification process should be stored into a flag to be used by other routines in the application.

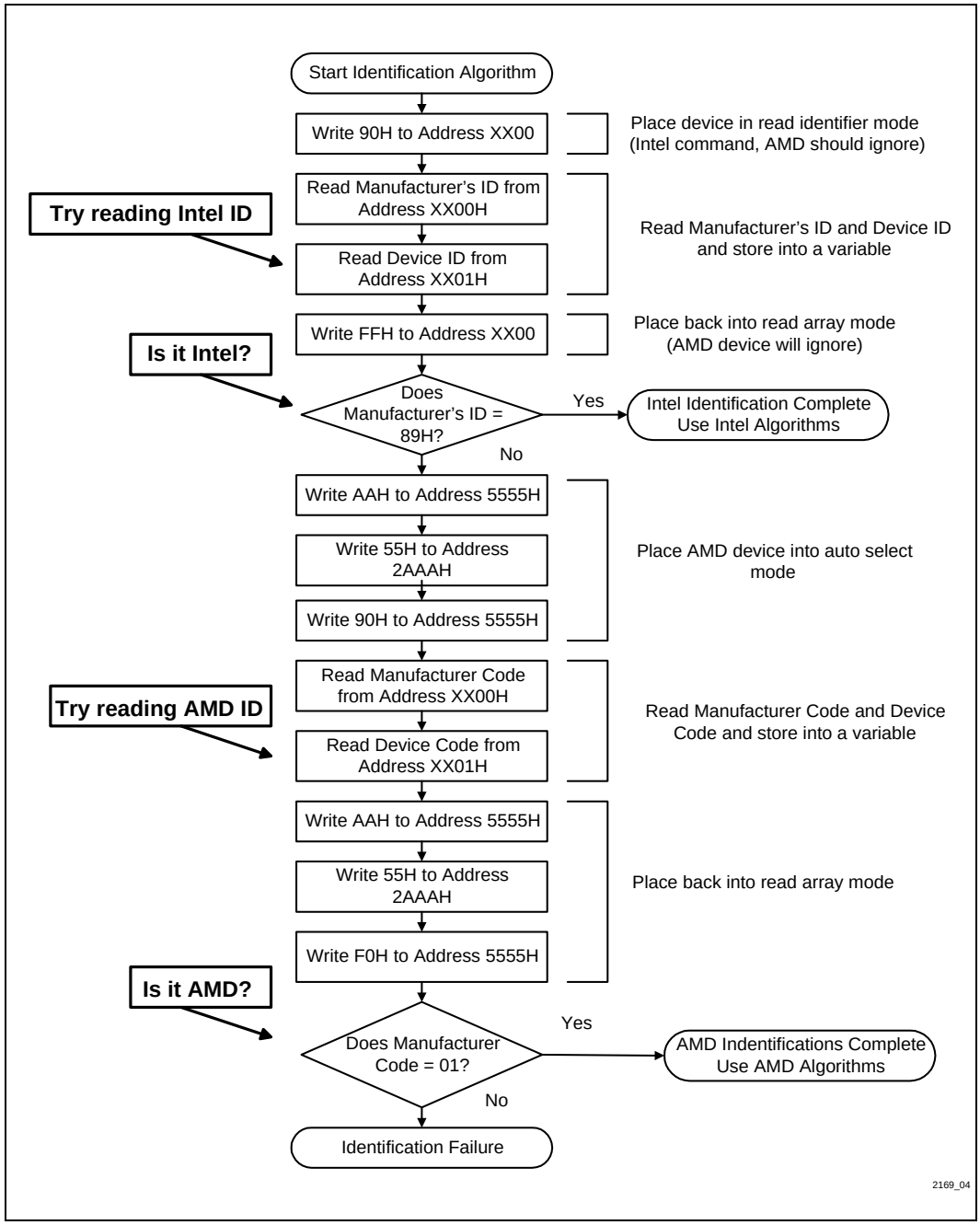

Figure 4. Intelligent ID Algorithm

2.5 Command Sequences

The Intel and AMD command sets are very different. On one hand, Intel commands are completed in two bus write cycles, and the only addresses involved are those directly related to the operation at hand. On the other hand, the AMD command set uses from two to six bus cycles for various commands, and most of the commands involve alternately switching the addresses to different locations. The two command sets are shown in Appendix B.

The key to accommodating the two different command sets is to distinguish the two different parts using the intelligent identifier algorithm discussed in Section 2.3. to set a flag indicating the device being used in that particular system. The flag should enable the software controlling the flash to execute the command sequence appropriate to the installed flash component.

A suggested way of implementing the separate command sequences is to use a case statement or If/Then series to check the flag value before the execution of any flash command. Depending on the value of the flag, a different sequence would be executed.

2.6 Block Locking

Intel and AMD use different locking schemes on their flash devices. Intel supports locking on the Boot Block only. This is controlled by signal levels on the RP# and WP# inputs. None of the other blocks can be locked (except by grounding V_{PP}, which effectively locks the entire device). AMD devices allow any combination of blocks to be locked, but the "marking" mechanism is similar to first-generation flash or EPROM programming techniques, requiring 12V applied to an address pin with manual pulse counts. Raising RESET# to 12V then unlocks all blocks, and RESET# at 5V sets the locked state for marked blocks. With these requirements, it is unlikely that dynamic marking/unmarking of blocks for locking can take place in system using the AMD method.

To make both types of devices work in the same socket, the AMD device's boot block should be marked as locked. Other blocks should be left unlocked for compatibility with Intel devices. Under these conditions, both Intel and AMD devices should operate similarly. Raising Intel's RP# pin or AMD's RESET# pin to 12V will unlock the boot block. However, Intel devices can also control boot block locking with a logic level signal, WP#, that does not require a 12V voltage supply.

2.7 Main Block Sizes

The Intel 28Fx00 and AMD 29Fx00 are both boot block architectures containing similar boot sections with identically sized boot, parameter, and small main blocks. However, the rest of the device is divided into main blocks of 64 KB (AMD) or 128 KB (Intel).

In some designs, the block size may not matter. One such case is if the software treats the entire flash device as one whole space and does not use the block scheme. However, software designs which depend on specific block sizes may need to be modified to work with the Intel blocking scheme, which provides the common denominator block size, 128 KB.

On the AMD side, the 64-KB blocks will need to be combined in pairs to produce 128-KB virtual blocks. The usage of "virtual" here means that to the software using the flash, it will only see a 128-KB symmetrically blocked space. The software can be thought of in two segments: an application that stores data to the flash device, and a driver that talks to the flash device on behalf of the application software. The application must be designed to use the virtual 128-KB block size and to call the driver segment for any write operations to the flash device. When erasing a virtual block, the driver translates that into the two physical blocks composing that virtual block and erases all component blocks.

The driver's combining algorithm, shown in Figure 5, works as follows: if the software wants to erase virtual block #n, then erase block n for an Intel part (i.e., no translation is needed for the Intel part, since no blocks need to be combined) or n and n-1 for an AMD part (since two of the AMD device's blocks need to be combined).

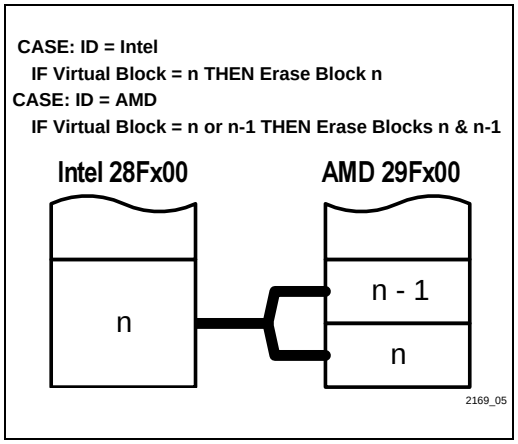

Figure 5. Main Block Combining Algorithm

APPENDIX A
INTEL – AMD FLEX SOCKET PRODUCT CORRESPONDENCE

5V ± 5% or 5V ± 10% Mode

Intel		AMD	
Part Name	**Description**	**Part Name**	**Description**
28F200B5	2M, Smart 5, 44-PSOP, 48-TSOP	29F200	2M, 5V-Only, 44-PSOP, 48-TSOP
28F400B5	4M, Smart 5, 44-PSOP, 48-TSOP	29F400	4M, 5V-Only, 44-PSOP, 48-TSOP
28F800B5	8M, Smart 5, 44-PSOP, 48-TSOP	29F800	8M, 5V-Only, 44-PSOP, 48-TSOP

2.7–3.6V (BE/CE) or 3.0-3.6V (BV/CV) Mode

Intel		AMD	
Part Name	**Description**	**Part Name**	**Description**
28F002BE	2M, SmartVoltage, 40-TSOP, 2.7-3.6V Read	not available	
28F002BV	2M, SmartVoltage, 40-TSOP, 3.0-3.6 Read		
28F200CE	2M, SmartVoltage, 48-TSOP, 2.7V Read	29LV200	2M, 3V-Only, 48-TSOP
28F200CV	2M, SmartVoltage, 48-TSOP, 3.0-3.6 Read		
28F004BE	4M, SmartVoltage, 40-TSOP, 2.7V Read	29LV004	4M, 3V-Only, 40-TSOP
28F004BV	4M, SmartVoltage, 40-TSOP, 3.0-3.6 Read		
28F400CE	4M, SmartVoltage, 48-TSOP, 2.7V Read	29LV400	4M, 3V-Only, 48-TSOP
28F400CV	4M, SmartVoltage, 48-TSOP, 3.0-3.6 Read		
28F008BE	8M, SmartVoltage, 40-TSOP, 2.7V Read	29LV008	4M, 3V-Only, 40-TSOP
28F008BV	8M, SmartVoltage, 40-TSOP, 3.0-3.6 Read		
28F800CE	8M, SmartVoltage, 48-TSOP, 2.7V Read	29LV800	4M, 3V-Only, 48-TSOP
28F400CV	8M, SmartVoltage, 48-TSOP, 3.0-3.6 Read		

APPENDIX B
INTEL – AMD FLASH COMMAND SEQUENCE COMPARISON

Command Function	Intel Command Sequence	AMD Command Sequence
Read Mode	XXXXH/FFH	XXXH/F0H
Read ID	XXXXH/90H	5555H/AAH, 2AAAH/55H, 5555H/90H
Program	Addr/40H, Addr/Data	5555H/AAH, 2AAAH/55H, 5555H/A0H, Addr/Data
Erase	Blk Addr/20H, Blk Addr/D0H	5555H/AAH, 2AAAH/55H, 5555H/80H, 5555H/AAH, 2AAAH/55H, Blk Addr/30H
Erase Suspend	XXXXH/B0H	XXXXH/B0H
Erase Resume	XXXXH/D0H	XXXXH/30H

NOTES:

1. Commands are given in the format Address/Data (in hexadecimal notation) above. This indicates the address that must be on the address bus and the data that must be on the data bus when the write pulse latches them in. For example, 5555H/90H would mean that the address 5555H must be applied to the flash address pins, and 90H to the data bus, when WE# goes low (or CE# for CE-controlled writes).

2. X = Don't care.

APPENDIX C
ADDITIONAL INFORMATION(1,2)

Order Number	Title
290599	*Smart 5 Boot Block Flash Memory Family 2, 4, 8 Mbit*
290531	*2-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet*
290530	*4-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet*
290539	*8-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet*
292154	*AB-60 2/4/8-Mbit SmartVoltage Boot Block Flash Memory Family Overview*
292194	*AB-65 Migrating Designs from SmartVoltage Boot Block to Smart 5 Flash*

NOTE:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.