AP-642

APPLICATION NOTE

Designing for Upgrade to Smart 3 Advanced Boot Block Flash Memory

March 1997

Order Number: 292200-001

CONTENTS

REVISION HISTORY

Number	Description
-001	Original version

1.0 INTRODUCTION

The new Smart 3 Advanced Boot Block product offering, on Intel's state-of-the-art 0.4µ process, is an enhancement to the current Boot Block product line.It introduces some new features that enable additional functionality and ease of design. This application note focuses on the technical differences between the current SmartVoltage (SVT) Boot Block and the Smart 3 Advanced Boot Block (B3) products.

This document is applicable for 4-Mbit and 8-Mbit densities. Section 2 covers the feature set of the new Advanced Boot Block. Analysis of electrical specifications and design recommendations for dual design (or upgrading) of SmartVoltage and Advanced Boot Block follows in Section 3.

2.0 SMART 3 ADVANCED BOOT BLOCK OVERVIEW

The new 4-, 8- and 16-Mb Advanced Boot Block products are designed for low voltage (2.7V–3.6V) applications. It supports functionality found on existing products and adds new capabilities driven by market requirements and technology break-throughs.

However, some SVT features were removed to enable improved low voltage support. Advanced Boot Block products do not support a) 5V operation and b) RP# block locking. All command sequences and modes of operation are identical to the SmartVoltage Boot Block. In addition, the new Advanced Boot Block flash memory family features:

- 2.7V–3.6V read, program and erase operation
- Enhanced parameter blocking
- Fast program suspend to read
- Fast erase suspend to program or read
- 1.8V I/O capability
- Advanced ETOX™ V 0.4µ lithography process technology

These architectural enhancements reduce device power consumption by more than 35% compared to previous flash products (refer to *AP-641 Achieving Low Power with Smart 3 Advanced Boot Block*). Furthermore, they enable code and data storage within a single flash device.

2.1 2.7V–3.6V Operation

Smart 3 Advanced Boot Block products offer 120 ns read operation over the entire range of 2.7V to 3.6V and across the full extended temperature range. This high-speed, low-voltage operation reduces power consumption for battery-powered devices such as cellular phones and other personal communications products. Typical [T = +25°C, nominal V_{CC}/V_{CCQ}] read and standby currents are 10 mA (at 5 MHz) and 30 µA respectively. For more extended battery life, the deep power-down feature reduces the device current to 1 µA typical. Of course, if higher speed programming is desired during manufacturing, a 12V option is still provided.

2.2 Enhanced Parameter Blocking

The Advanced Boot Block product is architected with eight 8-KB parameter blocks; the remainder of the array is divided into 64-KB blocks (Figure 1). This blocking is a superset to the current SmartVoltage blocking while maintaining the same block locking capability. Driving WP# to V_{IL} locks the upper two parameter blocks in the top configuration (lower two parameter blocks in the bottom configuration).

Although SmartVoltage and Advanced Boot Block both lock the upper (or lower) 16 KB of the flash, the two devices are partitioned differently. For SmartVoltage devices, a single program or erase command changes the contents of the lockable 16-KB block, whereas for B3 products, two program or erase commands are needed to change the contents of the lockable 8-KB blocks. Further, the remaining parameter blocks of the Advanced Boot Block map to a portion of the 96 KB block of SmartVoltage devices. These differences in blocking require software modifications beyond merely reconciling device ID differences (see Appendix A).

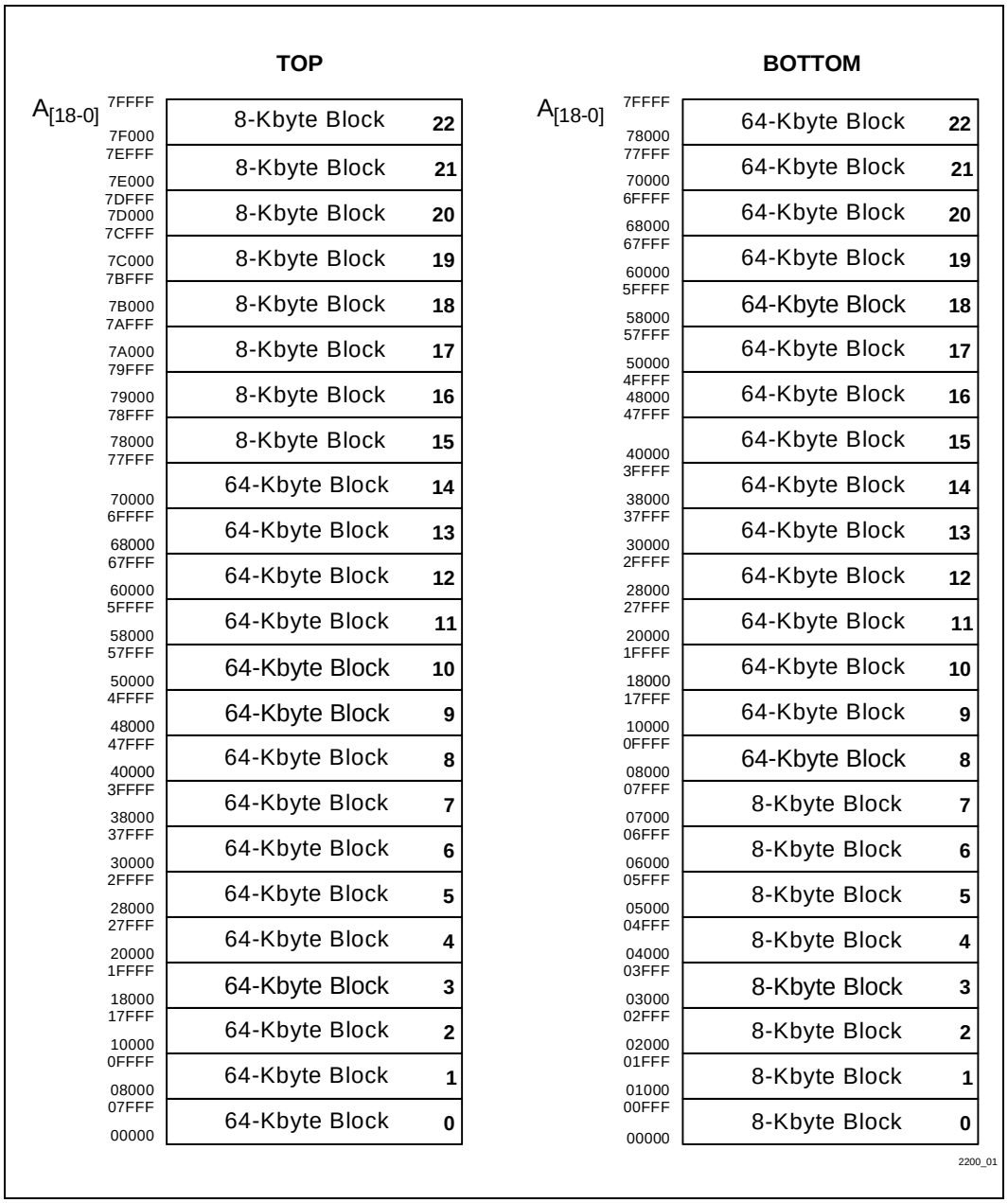


Figure 1. Blocking for the 8-Mbit Advanced Boot Block

2.3 Erase Suspend

Since flash memory erases on block boundaries, block size is an important part in data storage and update. Although the Advanced Boot Block has optimized 64-KB blocks, a code or data request may preempt an erase operation in progress. The erase suspend command allows suspension of an erase operation in order to read or program the flash. This means important data interrupts do not have to wait to be serviced. This functionality can be integrated into the system software for simplified implementation.

2.4 Program Suspend

Many applications require real time data updates or the ability to read code while another background operation is taking place. This has been previously impossible with all flash devices because a program operation could not be interrupted. The addition of this feature to the Advanced Boot Block makes it an ideal choice for such functions as software read-while-write and just-in-time code reads to service critical interrupts. Now both an erase and program operation can be suspended to perform multiple read operations.

2.5 1.8V I/O Capability

The major advantage of personal communication devices is convenience. For this reason, personal communication devices tend to be battery dependent. The need for lower voltages is easily understood in this paradigm since it directly relates to battery life. A significant portion of the voltage consumption the flash requires goes to driving the outputs of the device. If this were reduced, the battery life can be significantly improved. This is the benefit of 1.8V I/O capability.

Advanced Boot Block products provide a V_{CCQ} pin for controlling the input and output voltage level. The device still requires a V_{CC} of 2.7V–3.6V in order to function, but a separate, lower voltage supply can be used to reap lower power operation and longer battery life. V_{CCQ} can range from 1.8V to 2.2V or 2.7V–3.6V and the V_{IH} of the device is defined as V_{CCQ}-0.2V. Note the dependence on V_{CCQ} rather than V_{CC}. V_{OH} is also measured with respect to V_{CCQ}: $V_{OH} = V_{CCQ}–0.1V$. Typical [T = +25°C, nominal V_{CC}/V_{CCQ}] read and standby currents are 8 mA (at 5 MHz) and 30 µA.

3.0 SmartVoltage AND ADVANCED BOOT BLOCK COMPATIBILITY

As highlighted in the previous section, there are features on the Advanced Boot Block that are not available in the current SmartVoltage product family. There are several items to consider when designing a system to be SmartVoltage and Advanced Boot Block capable:

- pinout
- device ID
- 5V/12V operation
- block locking
- AC/DC specifications
- reset operations

3.1 Pinout

The SmartVoltage Boot Block and Advanced Boot Block are very similar in pinout. For the 48-lead TSOP package, there is only one pin difference between the two products:

Table 1. Pinout Differences for 48-Lead TSOP

Pin	SmartVoltage	Advanced BB
47	BYTE#	V_{CCQ}

Because of the low voltage capability of V_{CCQ}, designs that desire “drop-in” cross-functionality have to consider a jumper for this pin (see Figure 2). If BYTE# is hardwired to GND for x8 operation, a jumper is necessary for Advanced Boot Block upgradeability. To determine if a design requires a jumper, consult the subsequent tables.

If Design Has. . .	Then. . .
BYTE# = GND	need BYTE#/V_{CCQ} Jumper
Pull-up Resistor on BYTE#	need to eliminate pull-up and drive V_{CCQ} to proper voltage levels
RP# hardwired to 12V	need a jumper for 2.7V–3.6V/12V
V_{CC} = 5V	need to either change power supply or step voltage to valid levels

Table 2 below summarizes the jumper requirements. Regardless of the present voltage model, if future designs are going to use 1.8V I/O, a jumper is absolutely required. **Insure the trace width of V_{CCQ} is adequate to handle the current.** Keep in mind if 1.8V is not being used, V_{CC} and $V_{CC}Q$ **must** share a common supply; otherwise device operation is not guaranteed.

Table 2. BYTE# and V_{CCQ} Jumper Options

Current Design	Future Design	Jumper?
5V V_{CC}	5V V_{CC}	INVALID
5V V_{CC}	3.3V V_{CC}	Yes
3.3V V_{CC}	3.3V V_{CC}	No
2.7V–3.6V V_{CC}	2.7V–3.6V V_{CC}	No
2.7V–3.6V V_{CC}	1.8V–2.2V I/O	Yes

Note there is no 5V capability on the Advanced Boot Block products. Any design that uses or plans to use 5V V_{CC} will not be able to upgrade to Advanced Boot Block flash devices. Smart 5 devices offer 5V read, program and erase capability. Also note that because V_{CCQ} takes the place of BYTE# in Advanced Boot Block devices, there is no x8/x16 selectability. The 48-lead TSOP package is x16 only.

The lack of 5V capability on Advanced Boot Block is not limited to the V_{CC} input. V_{PP} is also not 5V "tolerant." In addition to a BYTE# jumper, a V_{PP} jumper will also be necessary if the present design is a 5V design. Figure 2 depicts the jumper options necessary when designing for both SmartVoltage and Advanced Boot Block devices.

3.2 Device ID

The device ID for the SmartVoltage products is different from that of the Advanced Boot Block devices. Whatever software is currently being used will need to identify which flash device is in the system. Table 3 lists the device IDs for the 8-Mb and 4-Mb devices. The manufacturer's ID remains the same for all products (0089H).

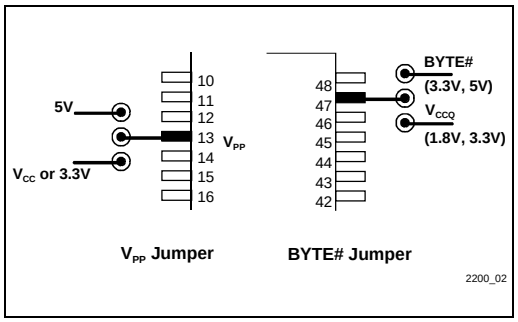


Figure 2. 48-Lead TSOP Jumper Option for V_{PP}, BYTE# and V_{CCQ}

Table 3. SmartVoltage and Advanced Boot Block Device IDs

		8-Mbit		4-Mbit	
		SVT	B3	SVT	B3
x16	Top	889CH	8892H	4470H	8894H
	Bottom	889DH	8893H	4471H	8895H

3.3 5 Volt/12 Volt Operation

Advanced Boot Block products are not 5V tolerant. Any I/O pin that is connected to a 5V supply for a duration longer than specified in the Absolute Maximum Ratings of the device could cause permanent damage to the flash memory. Device operation is not guaranteed under this condition.

If upgrading from a 5V environment to a 3V environment, insure all inputs and outputs are properly designed for the lower voltage tolerance. Also, do not forget the V_{CCQ}/BYTE# and V_{PP} jumpers that are required for proper operation of Advanced Boot Block devices in SmartVoltage systems.

The 12V program/erase capability of the Advanced Boot Block is intended for limited use in a production environment. Hardwiring 12V to V_{PP} is **not** permitted. 12V program and erase operations have a direct correlation to block cycling capability. Consult the product datasheet for cycling derating at 12V.

3.4 Block Locking

SmartVoltage Boot Block devices offer two pins for locking the boot block:

- RP# is the master unlock input (12V tolerant)
- WP# is 5V unlock input

For Advanced Boot Block devices, RP# is not 12V tolerant. Taking RP# to 12V is **not** allowed; it is outside the specified operating range for RP#. Doing so can cause permanent damage to the pin and prevent deep power-down functionality. The standard operating voltage for RP# is V_{IH} (which is dependent on V_{CCQ}); RP# = V_{IL} still puts the device into deep power-down mode and resets the flash memory. The V_{PP} pin can still be used to provide accidental program/erase protection. V_{PP} = V_{IL} prevents any Program or Erase commands from being executed by the WSM.Consult the Absolute Maximum Ratings for the absolute voltage tolerance of RP# (and all other I/O pins).

WP# must be used to achieve locking and unlocking under all voltage conditions. WP# = V_{IL} locks all lockable blocks; WP# = V_{IH} unlocks all locked blocks. This pin must be driven and cannot be left floating. Again note that V_{PP} = V_{IL} can be used to provide full device protection from spurious writes.

3.5 AC/DC Characteristics

Advanced Boot Block device specifications are either identical to or improved over SmartVoltage device specs. This means minimal impact to design environment after pinout and software issues have been properly handled. Due to its lower operating voltage, the Advanced Boot Block products are inherently lower power.

3.5.1 DC SPECIFICATIONS (V_{CCQ} = 2.7V–3.6V)

In this operating range, the DC specs for SmartVoltage are similar to that of Advanced Boot Block. Spec differences are highlighted in Table 4, below. The automatic power savings feature reduces I_{CCR} to approximately standby levels for static operation; in other words, after a read operation is completed, the current is automatically lowered even though CE# is still active.

Table 4. SmartVoltage and Advanced Boot Block 2.7V–3.6V Spec Differences

Symbol	Parameter	SmartVoltage		Advanced Boot Block		Unit	Conditions
		Typ	Max	Typ	Max		
I_{CCS}	V_{CC} Standby Current	50	110	20	50	µA	CMOS inputs
I_{CCD}	V_{CC} Deep Power-Down Current	0.2	8	1	10	µA	
I_{CCR}	V_{CC} Read Current	14	30	10	20	mA	5 MHz
I_{CCW}	V_{CC} Write Current	9	25	8	20	mA	V_{PP} = 12V
I_{CCW}	V_{CC} Write Current			8	20	mA	V_{PP} = 2.7–3.6V
I_{CCE}	V_{CC} Erase Current	9	25	8	20	mA	V_{PP} = 12V
I_{CCE}	V_{CC} Erase Current			8	20	mA	V_{PP} = 2.7–3.6V
I_{PPW}	V_{PP} Write Current	8	25	10	25	mA	V_{PP} = 12V
I_{PPW}	V_{PP} Write Current			15	40	mA	V_{PP} = 2.7–3.6V
I_{PPD}	V_{PP} Deep Power-Down Current	0.2	10	0.2	1	µA	

Table 4. SmartVoltage and Advanced Boot Block 2.7V–3.6V Spec Differences (Continued)

Symbol	Parameter	SmartVoltage		Advanced Boot Block		Unit	Conditions
		Min	Max	Min	Max		
V_{IL}	Input Low Voltage	–0.5	0.8	–0.4	0.4	V	
V_{IH}	Input High Voltage	2.0	V_{CC} ± 0.5	V_{CCQ} – 0.4		V	
V_{OL}	Output Low Voltage		0.45		0.1	V	
V_{OH}	Output High Voltage	V_{CC} – 0.4		V_{CCQ} – 0.1		V	CMOS inputs I_{OH} = –100 µA
V_{LKO}	V_{CC} Write/Erase Lock Voltage	2.0		1.5		V	

NOTES:
All specs shown are based on 16-Mb Advanced Boot Block. 8-Mb and 4-Mb specs may be different for some values. All specs are subject to change. Consult the datasheet for guaranteed specs.

3.5.2 DC SPECIFICATIONS (V_{CCQ} = 1.8V–2.2V)

Current SmartVoltage Boot Block products do not support this mode of operation. All specs delineating this mode are fully explained in the Advanced Boot Block datasheet. When designing to use this feature, it is important to make sure trace widths can handle the current load at this voltage. The voltage on the previous BYTE# pin is also critical for this mode of operation. The BYTE# jumper discussed earlier may be necessary to support both SmartVoltage and Advanced Boot Block.

3.5.3 AC READ SPECIFICATIONS (ALL MODES)

One of the major advantages of Advanced Boot Block over SmartVoltage is device wake-up time. This change (see table 5) is the only difference in read specifications between SmartVoltage and Advanced Boot Block.

Table 5. SmartVoltage and Advanced Boot Block AC Read Differences

Sym	Parameter	SVT	B3	Unit
		Max	Max	
t_{PHQV}	RP# to output delay	800	600	ns

3.5.4 AC WRITE SPECIFICATIONS (ALL MODES)

SmartVoltage devices specify separate CE#-controlled and WE#-controlled operations for program and erase. These specs have been combined for Advanced Boot Block Products. The wake-up time of the device is also different between SmartVoltage and Advanced Boot Block (see table 6). The next section details specific changes to the reset timings.

Table 6. SmartVoltage and Advanced Boot Block AC Write Spec Differences

Sym	Parameter	SVT	B3	Unit
		Max	Max	
t_{PHEL} t_{PHWL}	RP# at V_{IH} to CE# (WE#) low delay	800	600	ns

3.6 Reset Operations

Both SmartVoltage and Advanced Boot Block devices include an RP# pin which can be used as a RESET input. When RP# is toggled from V_{CC}-GND-V_{CC}, the flash memory is reset to read array mode. The minimum low pulse width necessary to fully reset the flash device, t_{PLPH}, is 100 ns. If t_{PLPH} is less than 100 ns, the device may still reset but this is not guaranteed.

RP# going low can also be used to abort program/erase operations. Existing SmartVoltage devices perform a hard interrupt, meaning the operations is abruptly halted and portions of the array will contain erroneous data and partially programmed or erased bits. Advanced Boot Block devices employ a more robust abort scheme: a clean abort is performed such that the device is only aborted at a known state within the internal write sate machine. This prevents partially programmed or erased bits.

This clean abort scheme introduces an additional delay when entering reset while program or erase operations are in progress. Although the minimum pulse width required for RP# is still 100 ns, the flash will not consume power-down current until a maximum of 20 µs after RP# is driven low. This time is a maximum since the exact point within the algorithm where termination will occur is application/abort dependent.

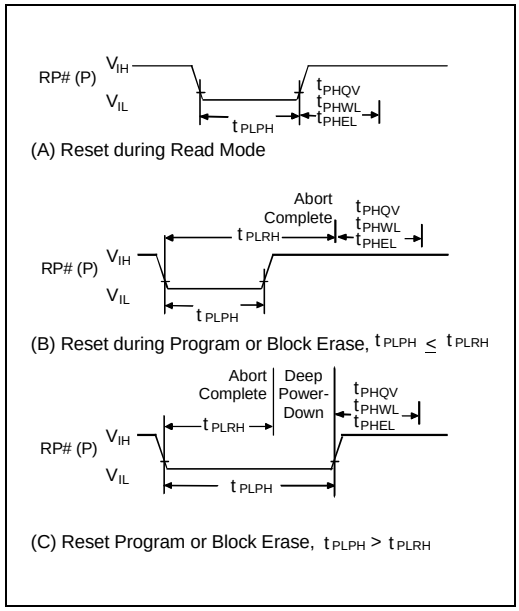


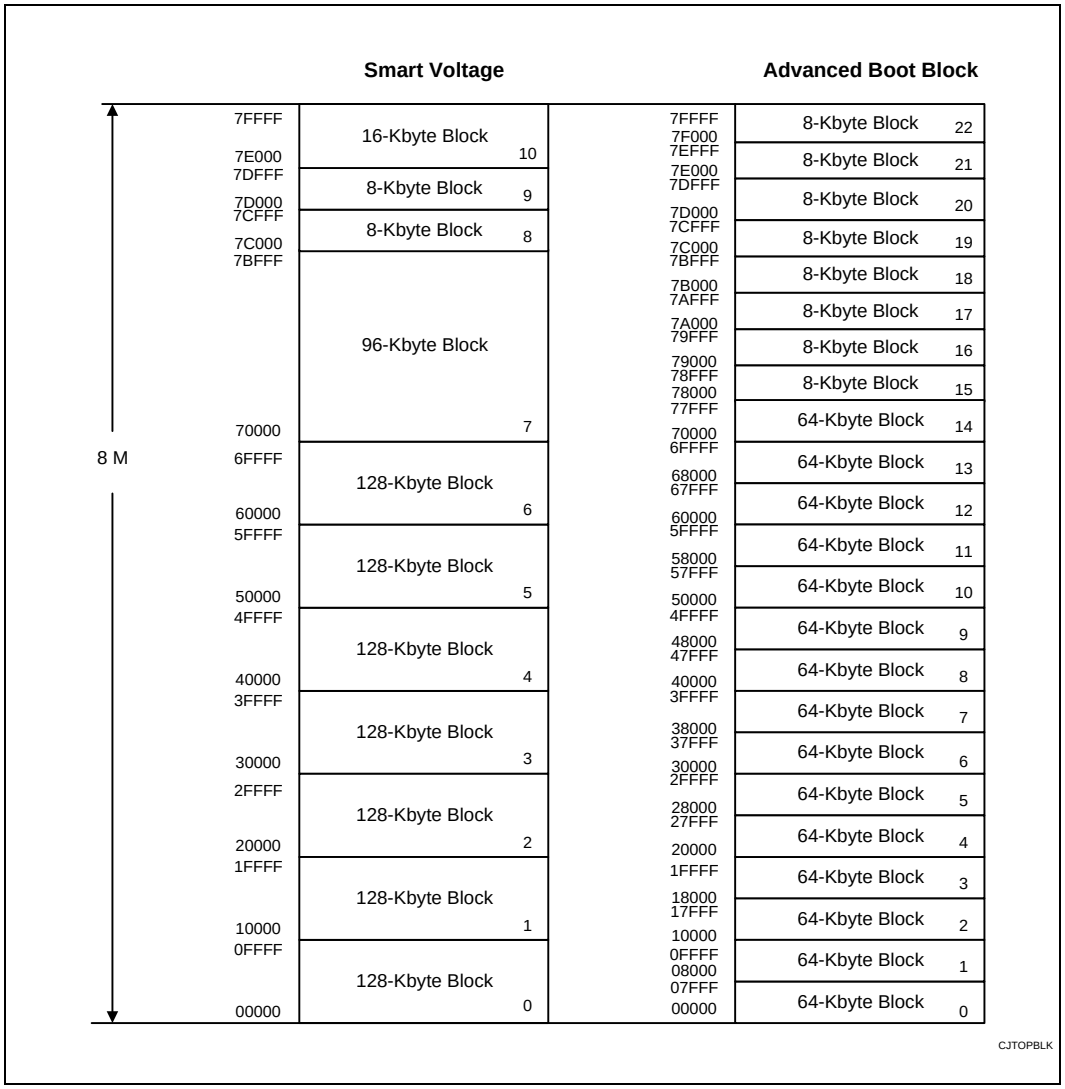
Figure 3. AC Waveform: Deep Power-Down / Reset Operation

RP# does **not** need to be kept low for the full 20 µs. It may be kept low for 100 ns (minimum) and then returned high. However, the device will not enter power-down until either (a) the program or erase operation has successfully aborted **or** (b) the 20 µs maximum time has expired, whichever occurs first. If RP# is toggled high-low-high for 100 ns, the flash will enter deep power-down after the pending operation has been successfully aborted and then immediately begin the wake up process, which is gated by t_{PHQV}. Regardless of whether power-down is entered following a program/erase abort or not, t_{PHQV} must still be met when coming out of power-down.

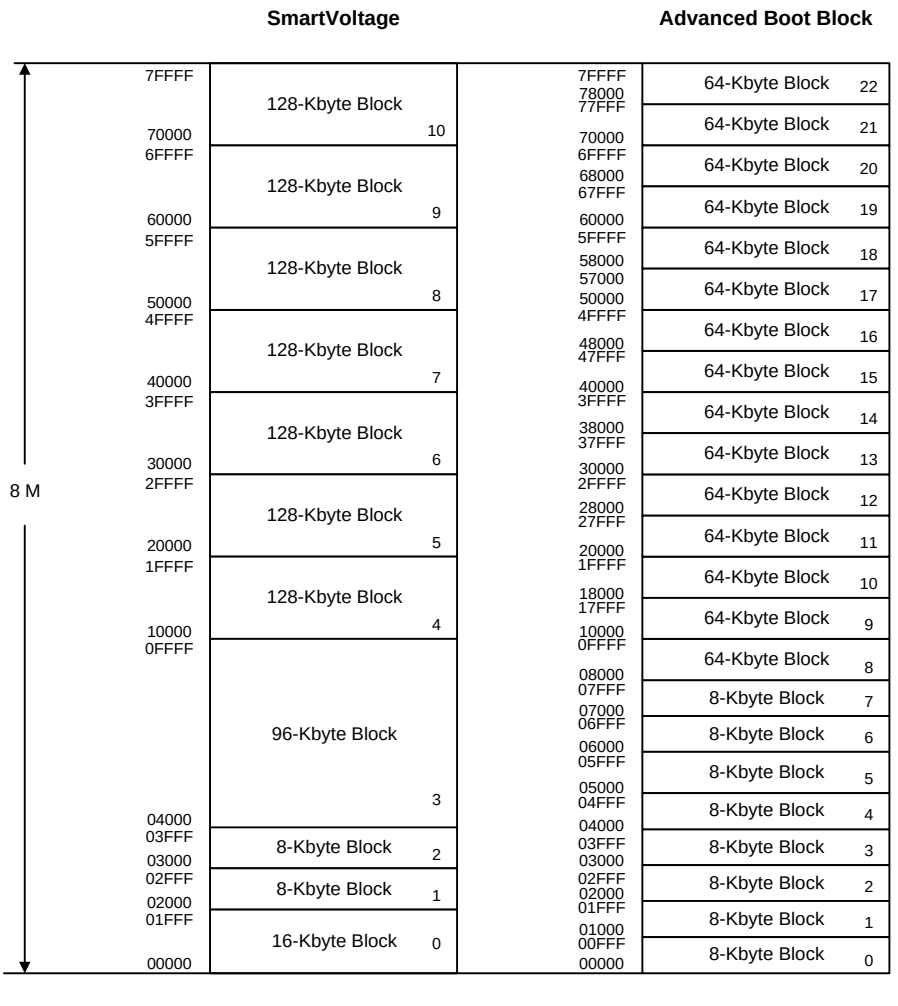
4.0 CONCLUSION

This document outlines necessary design steps when designing for both standard SmartVoltage devices and the new Advanced Boot Block architecture. It discusses everything from blocking to software to pin compatibility. Applications should be designed for compatibility with Advanced Boot Block products to ensure the most cost-effective solution.

APPENDIX A
BLOCK MAPPING OF SmartVoltage AND ADVANCED BOOT BLOCK FLASH MEMORY



8-Mbit Top Blocking



8-Mbit Bottom Blocking

APPENDIX B
ADDITIONAL INFORMATION(1,2)

Order Number	Document/Tool
210830	*1997 Flash Memory Databook*
290580	*Smart 3 Advanced Boot Block 4-Mbit, 8-Mbit, 16-Mbit Flash Memory Family* Datasheet
292199	*AP-641 Achieving Low Power with Smart 3 Advanced Boot Block*

NOTE:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.