AP-641

APPLICATION NOTE

Achieving Low Power with Advanced Boot Block Flash Memory

March 1997

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REVISION HISTORY

Number	Description
-001	Original version

1.0 INTRODUCTION

Portable applications such as cell phones, pagers, and global navigation systems, continue to demand lower power devices (e.g., flash and microcontrollers) to accommodate customer demand for longer battery life. This application note discusses how Intel's Smart 3 Advanced Boot Block devices have been designed for low power. It first looks at different modes a flash device operates in and how its power is calculated. A study of the variables that affect power consumption follows from these calculations. This analysis of the factors that affect power consumption shows how Intel's Smart 3 Advanced Boot Block (B3) 1.8V I/O option reduces power. Power comparisons in subsequent sections are made between the 8-Mbit Smart 3 Advanced Boot Block device (28F800B3) and the 8-Mbit SmartVoltage Boot Block device (28F800BE).

2.0 FLASH MODES OF OPERATION

At a given time, a flash device operates in one of the following modes:

1. **Active (or Read)**: Flash device is being read. Enabled when CE# and OE# are driven low and RP# is high.
2. **Program**: Flash device is being programmed. Enabled when CE# and WE# are driven low and RP# is high.
3. **Erase**: Flash device is being erased. Enabled when CE# and WE# are driven low and RP# is high.
4. **Standby**: Flash device is idle (outputs at high Z). Enabled when CE# transitions high and the power-down pin (RP#) remains high.
5. **Deep Power-Down**: Flash device is asleep. Enabled when RP# is driven low.

For most applications, the flash device is in active (read) or standby mode a majority of the time. The amount of time spent in each mode depends on the application. Section 4.4, *Active vs. Standby Mode* looks at the percent total power savings between the 28F800B3 (B3) and the 28F800BE (BB) as a function of the percent of time spent in these modes.

3.0 POWER EQUATIONS

The flash device can be separated into two sections: the core and the I/O. Figure 1 shows a representation of a flash device with the core and the I/Os separated. The total power consumption is the sum of the power consumed by the core and the power consumed by the I/Os. The operating mode of the device must be comprehended in the equations since the current consumption varies per mode. This application note focuses on active and standby power consumption. Program, erase, and deep power-down contribute little to flash power consumption when you consider the amount of time spent in these modes. Also note that power consumed through V_{PP} does not greatly impact the power calculations (the current is very small) when in active or standby mode and is therefore removed from the equations for simplifications.

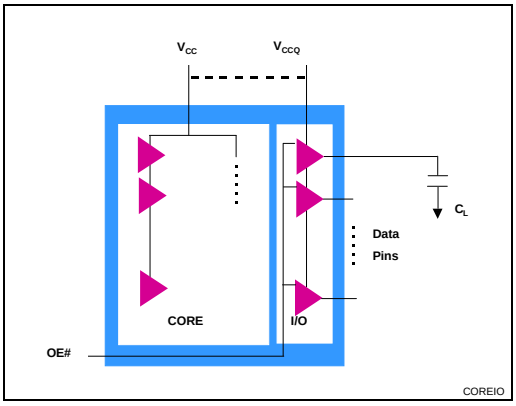

Figure 1. Representation of a Flash Device with Core and I/Os Separated

Therefore the total power is:

$$P_{total} = P_{core} + P_{I/O}$$

P_{core} is calculated as follows :

P_{core} = [(% of time spent in active mode) * (Power consumed by core in active mode(P_{active}core)]
+ [(% of time spent in standby mode) * (Power consumed by core in standby mode($P_{standby}$core)]

where:

$P_{active}core$ = read current * supply voltage

$= I_{CCR} * V_{core}$

$P_{standby}core$ = standby current * supply voltage

$= I_{CCS} * V_{core}$

$P_{I/O}$ is calculated as follows:

$P_{I/O}$ = [(% of time in active mode) * (Power consumed by I/Os in active mode($P_{active}I/O$)]
+ [(% of time spent in standby mode) * (Power consumed by I/Os in standby mode($P_{standby}I/O$)]

where:

$P_{active}I/O$ = load capacitance * frequency of I/Os switching * (I/O supply voltage)^2 * # of I/Os switching

$= C_L * f * (V_{I/O})^2$ * # of I/Os switching (16 for a x16 part)

$P_{standby}I/O = C_L * f * (V_{I/O})^2$ * # of I/Os switching

= 0 since the # of I/Os switching is 0

4.0 VARIABLES THAT AFFECT POWER CONSUMPTION

The equations defined in Section 3 reveal there are several variables that effect power consumption. This section looks at these variables: supply voltage, load capacitance, frequency, and the percent time spent in active vs. standby mode, in greater detail.

4.1 Supply Voltage

The equations for power shows a linear relationship between power and supply voltage for the core power and a square relationship between power and supply voltage for I/O power. Reducing the supply voltage will proportionally reduce the total power. A comparison is made below of the power consumption of the Smart 3 Advanced Boot Block (B3) with the SmartVoltage Boot Block (BE) for two different supply voltage options: $V_{CC} = V_{I/O} = 3.6V$ and $V_{CC} = V_{I/O} = 2.7V$, holding the following constant:

1. Load capacitance = 50 pF
2. Frequency = 8.33 MHz. This corresponds to a 120 ns access time with reads being performed continuously (see Section 4.3 for details).
3. The amount of time spent in active mode = 10% and the amount of time spent in standby mode = 90%.

From this analysis, an understanding will be gained into how much of the total power is attributed to the core and how much is attributed to the I/Os.

4.1.1 $V_{CC} = V_{I/O} = 3.6V$

Figure 2 shows the power comparison between the 28F800B3 (B3) and the 28F800BE (BB) components when both V_{CC} and $V_{I/O}$ are at 3.6V. When V_{CC} and $V_{I/O}$ are equal the power difference is significant only in the core. The I/O power consumption is the identical for both devices under these conditions. Also note that the amount of power consumed by the I/Os is greater than that of the core. The total power savings is 10% even though the I/O power is the same for both devices. This is the result of a reduced I_{CCR} (10 mA typical for B3 vs. 14 mA for BB) which decreases the active core power.

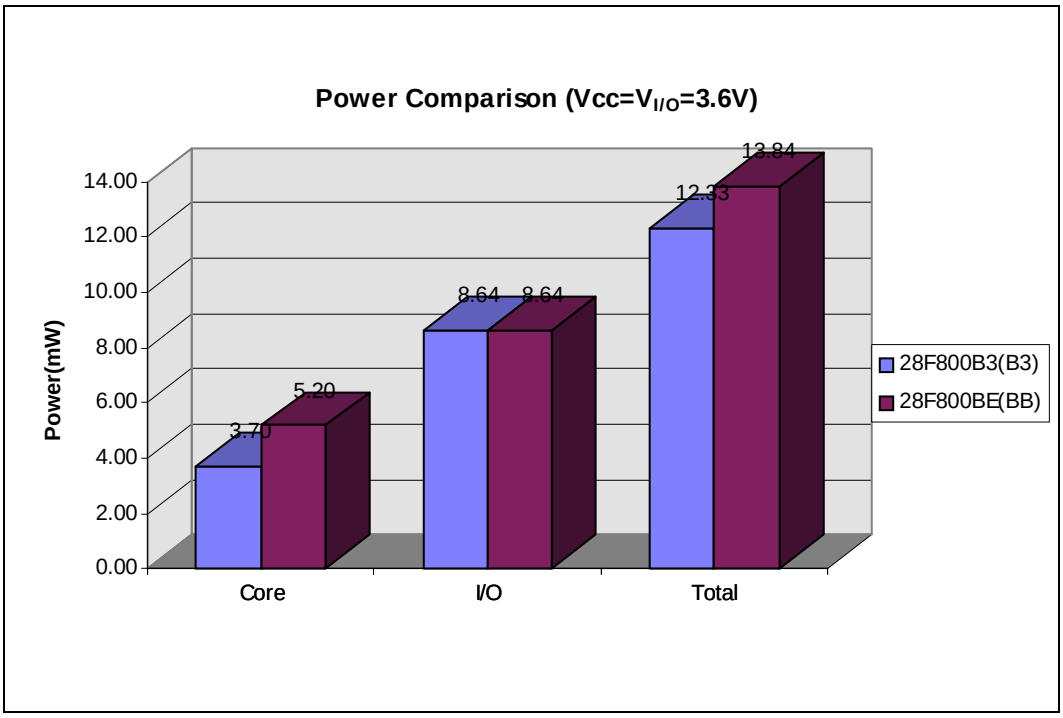

Figure 2. Power Comparison Showing Core, I/O and Total Power (V_{CC} = $V_{I/O}$ = 3.6V)

Smart 3 Advanced Boot Block:

$P_{total} = P_{core} + P_{I/O}$

P_{core} = (% of time spent in active mode) * I_{CCR} * V_{CC}
+ (% of time spent in standby mode) * I_{CCS} * V_{CC}

= 0.1 * 10 mA * 3.6V + 0.9 * 30 µA* 3.6V

= 3.6 mW + 0.0972 mW

= 3.697 mW

$P_{I/O}$ = (% of time spent in active mode) * C_L * f * $(V_{I/O})^2$ * # of I/Os switching

= 0.1 * 50 pF * 8.33 MHz * $(3.6V)^2$ * 16

= 8.636 mW

P_{total} = 12.33 mW

SmartVoltage Boot Block:

Using the above equations but changing I_{CCR} and the I_{CCS} to that of the Smart Voltage Boot Block, the total power consumption is:

P_{total} = 13.84 mW

Percent Total Power Savings:

% total
power savings = [total power consumed by the 28F800B3 – total power consumed by the 28F800BE]/total power consumed by the 28F800BE

= (13.84 mW – 12.33 mW)/ 13.84 mW

= 10.8% total power savings

4.1.2 V_{CC} AND V_{CCQ} = 2.7V

Figure 3 shows the power comparison between the B3 and the BB components when both V_{CC} and $V_{I/O}$ are at 2.7V. Again, only the core power is affected by changing the supply voltage. The I/O still consumes more power than the core. The total power savings is 12% even though the I/O power is the same for both devices.

Smart 3 Advanced Boot Block:

$P_{total} = P_{core} + P_{I/O}$

P_{core} = (% of time spent in active mode) * I_{CCR} * V_{CC} + (% of time spent in standby mode) * I_{CCS} * V_{CC}

= 0.1 * I_{CCR} * V_{CC} + 0.9 * I_{CCS}* V_{CC}

= 0.1 * 10 mA * 2.7V + 0.9 * 30 µA* 2.7V

= 2.7 mW + 0.0729 mW

= 2.773 mW

$P_{I/O}$ = (% of time spent in active mode) * C_L * f * $(V_{I/O})^2$ * # of I/Os switching

= 0.1 * 50 pF * 8.33 MHz * $(2.7V)^2$ * 16

= 4.858 mW

P_{total} = 7.63 mW

Smart Voltage Boot Block:

Calculations are similar to those for the Smart 3 Advanced Boot Block:

P_{total} = 8.76 mW

Calculations for Percent Total Power Savings

% total
power savings = [total power consumed by the 28F800B3 – total power consumed by the 28F800BE]/total power consumed by the 28F800BE

= (8.76 mW – 7.63 mW)/8.76 mW

= 12.8% total power savings

The calculations above show that when the core and I/O share a common supply, changes in the power supply only affect the core power consumption. Also, I/O power consumption is typically higher than the core. Section 5 discusses how the Smart 3 Advanced Boot Block has been architected to provide significant reduction of I/O power consumption.

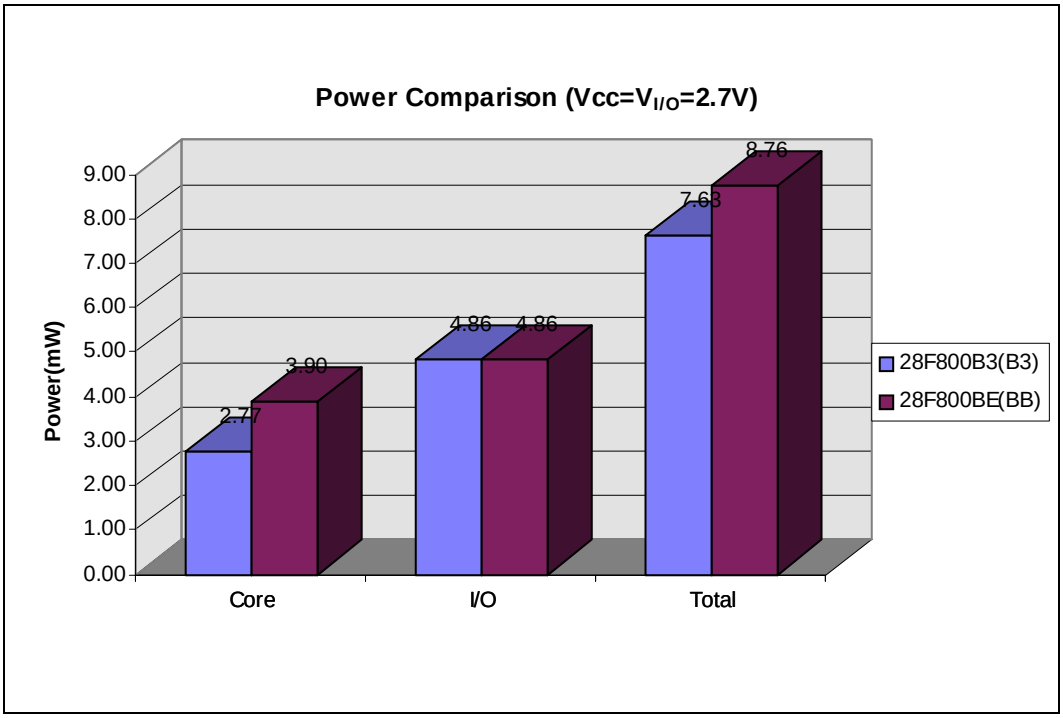

Figure 3. Power Comparison Showing Core, I/O and Total Power (V_{CC} = $V_{I/O}$ = 2.7V)

4.2 Load Capacitance

The load capacitance on the output only affects the power of the I/Os when the flash device is in active mode. The power consumption is a function of the current needed to charge or discharge the load capacitance. For example, if the output is changed from a logic low to a logic high, a certain amount of current is required to charge the load capacitance. The larger the capacitance, the more current that is needed. Figure 4 shows the current source to charge the load capacitance. If the output is changed from a logic high to a logic low, the charge stored on the load capacitance is discharged through the buffer. Figure 5 shows the discharge path of the load capacitance.

From the equations in Section 3, the power of the I/Os in active mode varies linearly with the capacitance:

$$P_{active}I/O = C_L * f * (V_{I/O})^2 * \#\text{ of outputs switching}$$

Assuming that:

1. $V_{CC} = V_{I/O} = 2.7V$
2. Frequency = 8.33 MHz
3. The amount of time spent in active mode = 10% and the amount of time spent in standby mode = 90%.

Figure 6 shows a comparison between the power consumption of the B3 and the BB for different load capacitance.

Load capacitance has a second order effect on the overall power consumption. The previous section showed how I/O power is typically higher than core power. The linear relationship between power and load capacitance explains why changing load capacitance has a minimal effect on the I/O power consumption. Exploiting the square relationship between I/O power and I/O voltage will have a more profound effect on I/O power consumption.

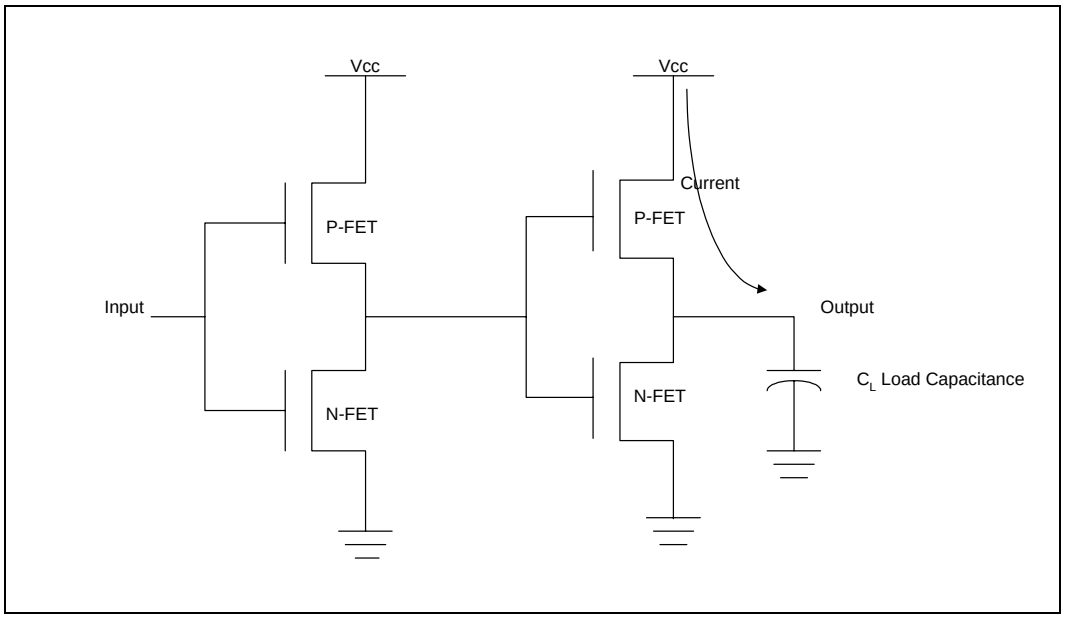

Figure 4. Load Capacitance Charging

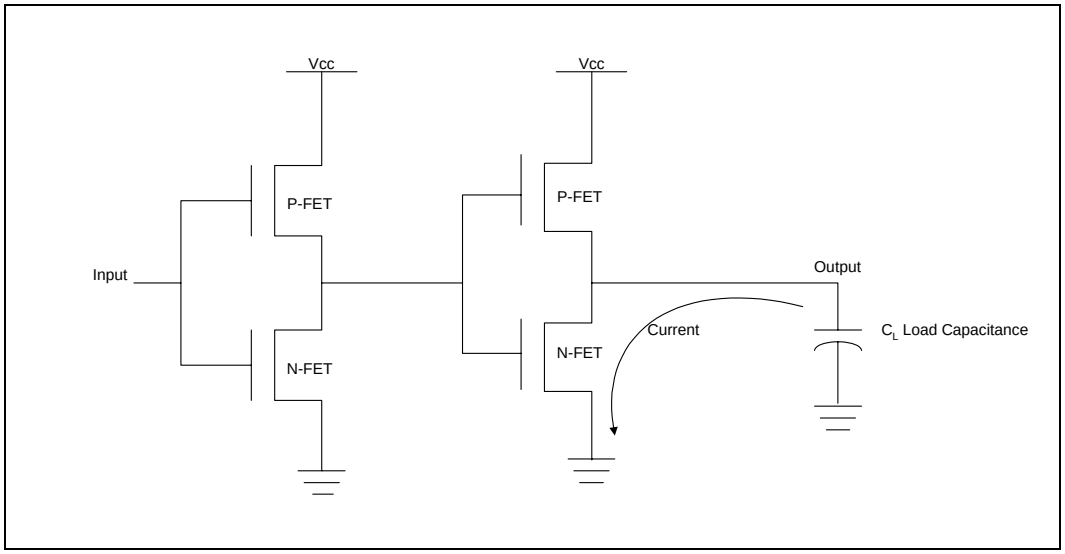

Figure 5. Load Capacitance Discharging

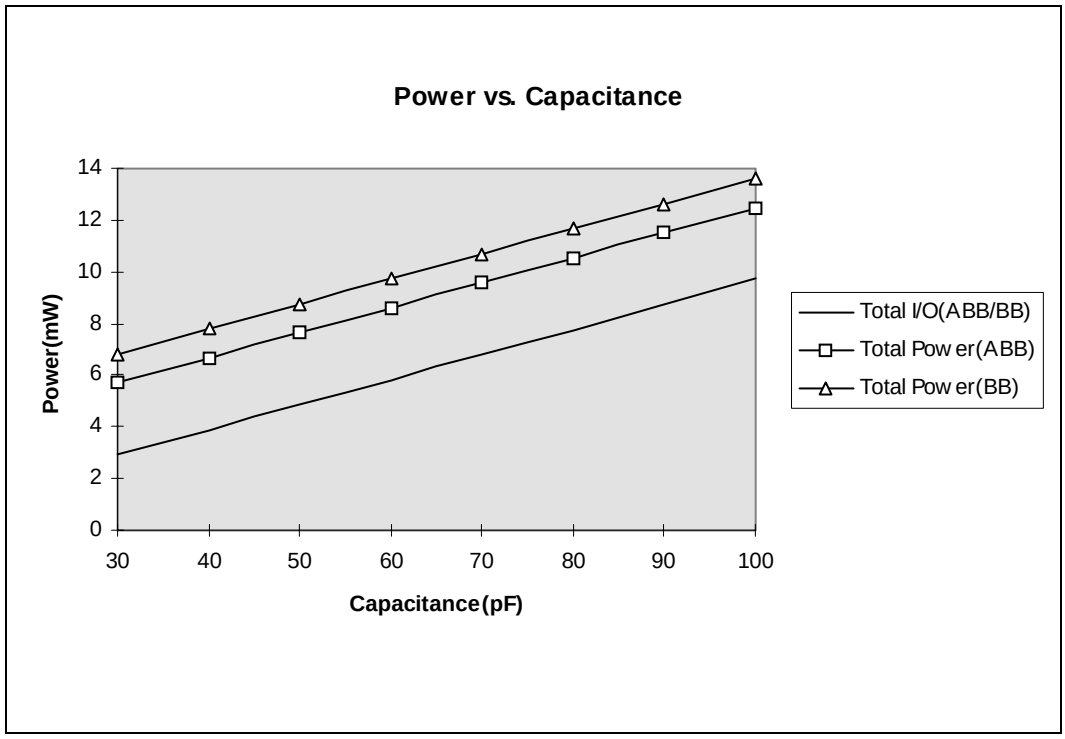

Figure 6. Power Affected Linearly by Change in Load Capacitance

4.3 Frequency

The frequency affects the power of the I/Os only when the flash device is in active mode. As the speed with which the load capacitance is charged or discharged increases, the current that is consumed also increases. This increased current increases the total power consumption. From the equations in Section 3:

$$P_{active}I/O = C * f * (V_{I/O})^2 * \#\text{ of outputs switching}$$

The equation reveals a linear relationship exists between the power of the I/Os in active mode and the frequency with which the I/Os are switching.

The maximum frequency that the I/Os can change is the device access time with reads performed continuously. For the B3 the access time is 120 ns resulting in a frequency of 8.33 MHz. Frequencies of less than the maximum represent systems in which read wait-states must be inserted for the flash device.

Figure 7 shows a comparison between the power consumption of the B3 and the BB. Again, the linear relationship diminishes the impact of frequency changes on I/O power consumption. Varying both linearly-dependent variables (i.e., load capacitance and frequency) will affect the amount of I/O power reduction. However, it would be more advantageous to capitalize on the square relationship between I/O power and I/O voltage.

A comparison is made between the power consumption of the B3 and the BB. Figure 7 shows that the I/O power and the total power of both devices are affected linearly by the change in frequency. The graph in Figure 7 assumes:

1. $V_{CC} = V_{I/O} = 2.7V$
2. Load Capacitance = 50 pF
3. The amount of time spent in active mode = 10% and the amount of time spent in standby mode = 90%

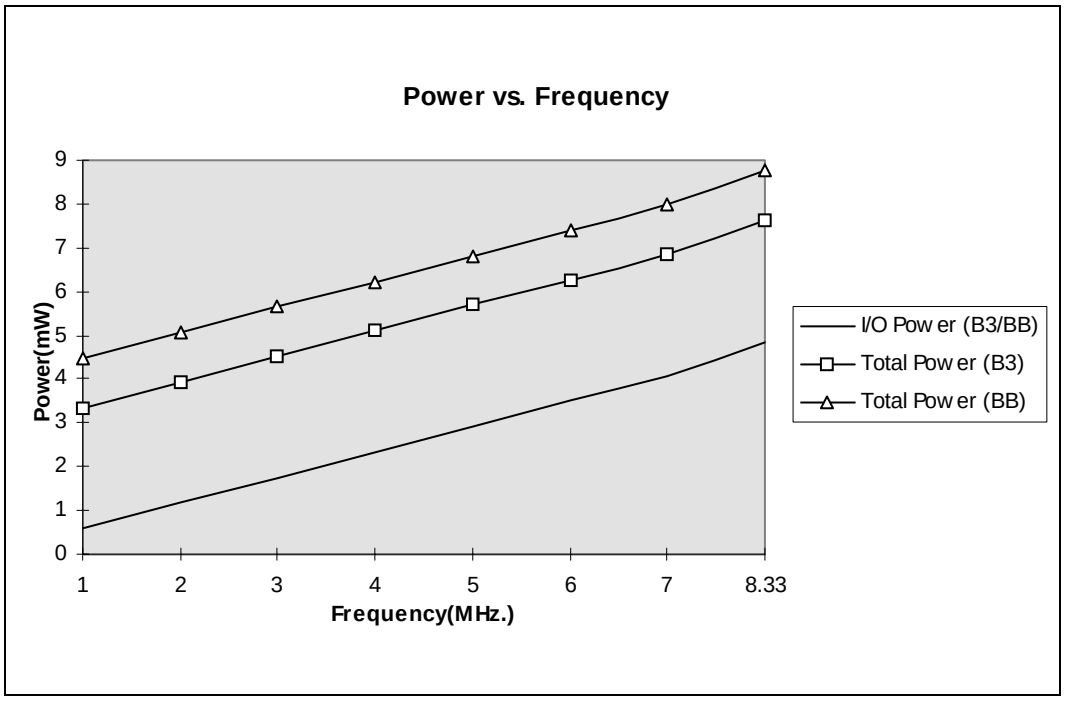

Figure 7. Power Affected Linearly by Change in Frequency

4.4 Active Mode vs. Standby Mode

From the calculations in Section 4.1.1 and 4.1.2 the following assertions were made:

1. For V_{CC} = $V_{I/O}$ = 3.6V, the percent total power savings = 10% for the B3 compared to the BB (90% standby, 10% active)
2. For V_{CC} = $V_{I/O}$ = 2.7V the percent total power savings = 12% for the B3 compared to the BB (90% standby, 10% active)

Applications spend varying amounts of time in active and standby modes. Often a correlation is made between the amount of time spent in standby and the total device power consumption; however this is not always the case. Figure 8 shows the percent total power savings vs. the percent time spent in standby mode. Between 5% and 95% the percent of total power savings is virtually unchanged—the graph is linear in this range!

The reason for such a small impact can be found in the equations of Section 3 and the magnitudes of both the active and standby currents. The active power is calculated as:

$$P_{active}core + P_{active}I/O = (\%\ of\ time\ spent\ in\ active\ mode)\ [\ (I_{CCR} * V_{CC})] + [(C_L * f * (V_{I/O})^2 * \#\ of\ I/Os\ switching)]$$

The standby power is calculated as:

$$P_{standby}core = (\%\ of\ time\ spent\ in\ standby\ mode) * I_{CCS} * V_{CC}$$

The major factors that differentiate the two are:

1. The percent time spent in that mode (active or standby)
2. The current (I_{CCR} or I_{CCS})

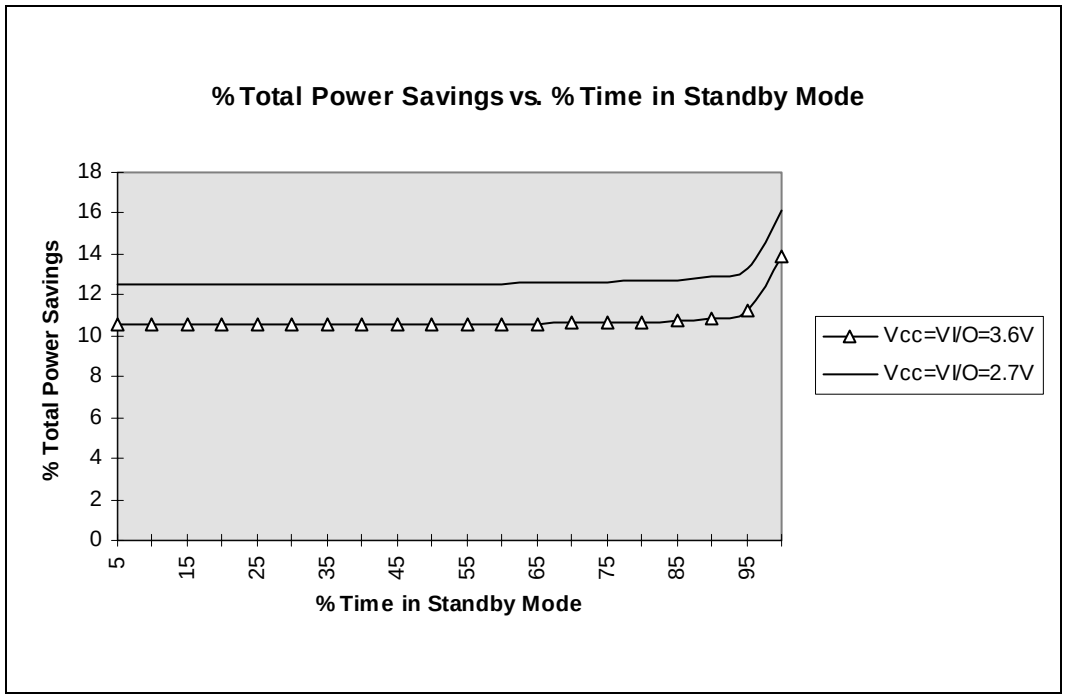

Figure 8. Percent Total Power Savings vs. Amount of Percent Time in Standby Mode

The standby current is three orders of magnitude less than the active current but the percent time spent in standby mode is about one order of magnitude more than the percent time spent in active mode (up to 91% standby mode). The percent total power savings remains fairly constant for both $V_{CC} = V_{I/O} = 3.6V$ and $V_{CC} = V_{I/O} = 2.7V$ up to 95% and only increases less than 5% from 95% to 99% (time spent in standby mode). **Therefore, the amount of time spent in standby mode vs. active mode does not significantly impact the percent total power savings.**

Two common applications and the percent of time each spends in active and standby mode is given below:

Cell phone:	95% standby, 15% active
Pager:	96.5% standby, 3.5% active

5.0 LOW POWER WITH SMART 3 ADVANCED BOOT BLOCK FLASH

Previous sections showed that I/O power can be significantly higher than core power. Unfortunately, existing flash memory devices do not address I/O power consumption. Intel's Smart 3 Advanced Boot Block is designed to reduce I/O power consumption. The device provides two voltage pins: V_{CC} for the core logic and V_{CCQ} for I/O drivers. This allows I/Os to be driven at lower voltages than the core, as low as 1.8V.

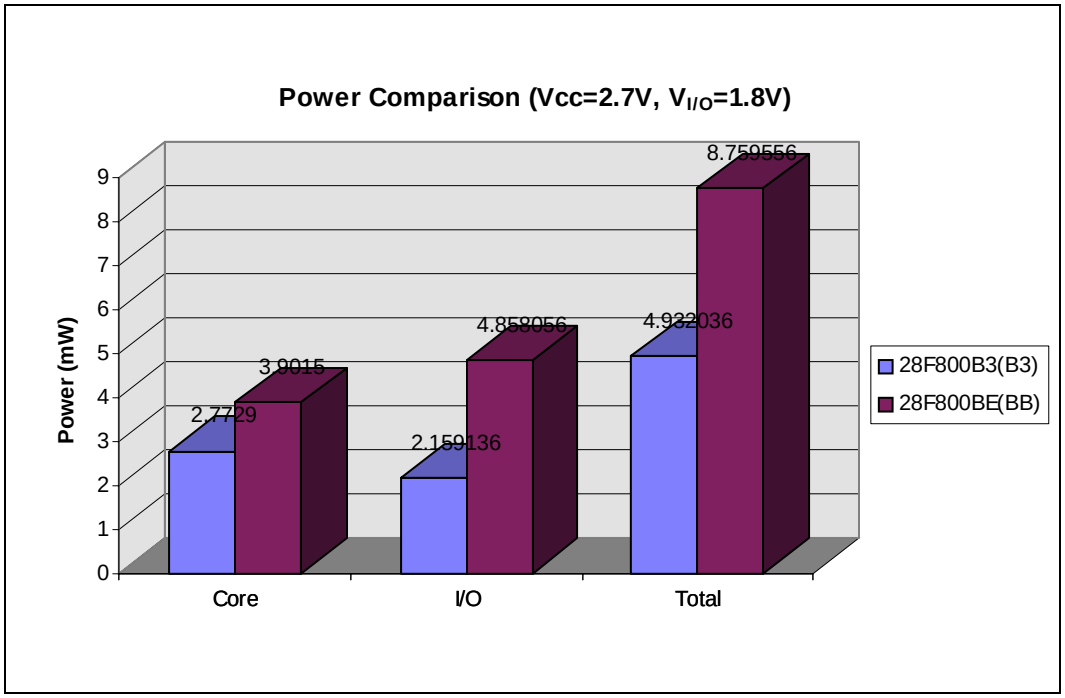

Figure 9. Power Comparison (V_{CC} = 2.7V, $V_{I/O}$ = 1.8V)

Figure 9 shows the power comparison between the B3 and the BB components when V_{CC} is at 2.7V and V_{CCQ} is at 1.8V. Note that the $V_{I/O}$ for the BB is 2.7V since this device does not have a 1.8V I/O option. A 35% total power savings can be realized with the 1.8V I/O option. The Smart 3 Advanced Boot Block takes advantage of the square relationship that exists between I/O power and I/O voltage. By reducing the I/O power consumption, the total power consumption is also reduced.

6.0 CONCLUSION

This application note explained the variables that affect power consumption in a flash device:

1. **Supply voltage:** A linear relationship exists between the total power and core power and a square relationship exists between the total power and I/O power.
2. **Load capacitance:** Linearly affects the I/O power and thus the total power consumption.
3. **Frequency:** Linearly affects the I/O power and thus the total power consumption.
4. **Amount of time spent in standby vs. active mode:** Percent total power savings is minimally impacted by the amount of time.

Intel's Smart 3 Advanced Boot Block with a 1.8V I/O option provides significant total power savings over existing flash memory.

APPENDIX A
ADDITIONAL INFORMATION(1,2)

Order Number	Document/Tool
210830	*1997 Flash Memory Databook*
290580	*Smart 3 Advanced Boot Block 4-Mbit, 8-Mbit, 16-Mbit Flash Memory Family* Datasheet