AB-65

APPLICATION BRIEF

Migrating SmartVoltage Boot Block Flash Designs to Smart 5 Flash

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CONTENTS

REVISION HISTORY

Number	Description
-001	Original version

1.0 INTRODUCTION

This application brief discusses the differences between SmartVoltage boot block flash memory products and the newer Smart 5 boot block products and covers the design considerations necessary to migrate designs to the lower cost Smart 5 products.

1.1 What Is Smart 5 Flash?

Smart 5 is a new voltage option for Intel SmartVoltage flash memories. Products supporting the Smart 5 option can read with V_{CC} at 5V and program and erase with V_{PP} at either 5V or 12V.

1.2 Why Use Smart 5 Flash?

Smart 5 products allow:

1. Simple single-supply designs with both V_{CC} and V_{PP} at 5V.
2. Fast factory programming with V_{PP} = 12V, which can save 20 cents/Mbit over single-supply flash.

Smart 5 products save you money with simplified designs, lower manufacturing costs, and the lowest cost SmartVoltage flash components.

2.0 MIGRATING DESIGNS FROM SmartVoltage

If a design does not require low-voltage operation, consider migrating to Intel's Smart 5 boot block flash. Smart 5 boot block products offer the same architecture as SmartVoltage boot block parts, but support only 5V V_{CC}. Designs requiring low-voltage operation should consider a SmartVoltage product instead.

Both product lines are similar in most features. The pinouts, Intelligent ID codes, block architectures, command sets, and timing specifications for the Smart 5 boot block products are all equivalent or better than their corresponding SmartVoltage parts. However, the 40-lead TSOP and 56-lead TSOP packages available in SmartVoltage are not supported on Smart 5; the 48-lead TSOP is recommended for designs converting from these packages. The SmartVoltage/Smart 5 product correspondence is listed in Appendix A.

The technical differences that exist will be discussed in the following sections.

2.1 Unified Write Specifications

The write timing specifications for Smart 5 products no longer distinguish between WE#-controlled and CE#-controlled write operations. Instead, both types of write operations have been unified into a single, simplified set of specs. This was possible because the

Table 1. SmartVoltage vs. Smart 5 Boot Block Feature Comparison

Feature	SmartVoltage	Smart 5
Process Technology	0.6µ ETOX™ IV	0.4µ ETOX™ V*
V_{CC} Read Voltage	2.7V–3.6, 3.0 ± 0.3V, or 5V ± 10%	5V ± 10%
V_{PP} Prog/Erase Voltage	5V ± 10% or 12V ± 5%	
Bus-Width	x8/x16 switchable (dynamic)	x8/x16 configurable (static)
Blocking (Top or Bottom boot locations available)	One 16k Boot Block Two 8k Parameter One 96k Main Block One or more 128k Main Block	
Locking	Boot Block lockable using WP# and/or RP# All other blocks protectable using V_{PP} switch	
Operating Temperature	Commercial or Extended	
Erase Cycling	100,000 cycles at Commercial Temperature 10,000 cycles at Extended Temperature	
Packages	40-L, 48-L, 56-L TSOP, 44-L PSOP	44-L PSOP, 48-L TSOP

* Initial production units of Smart 5 boot block products are on 0.6µ ETOX™ IV process technology.

setup and hold times of CE# and WE# relative to each other have been eliminated on both the SmartVoltage and Smart 5 boot block products.

This change is more in how the write timing specifications are presented in the datasheet, not in the timings themselves. The write timings for SmartVoltage and Smart 5 boot block parts are equivalent and compatible.

2.2 Byte-Word Mode Switching

SmartVoltage boot block parts supported dynamic, on-the-fly switching between byte (x8) and word (x16) mode using the BYTE# pin. The Smart 5 boot block products support static byte or word mode operation, but not switching during device operation. Word-byte mode must be configured using the BYTE# pin at device power-up or reset recovery and remain stable during operation. Consequently, the timing specifications associated with mode switching (t_{ELFL}, t_{ELFH}, t_{AVFL}, t_{FLQV}, t_{FHQV}, t_{FLQZ}) are not included in the Smart 5 boot block datasheet.

2.3 Reset Timing

Smart 5 products handle reset operations and timing differently from SmartVoltage boot block parts. Both require RP# to be low for a time t_{PLPH} in order to initiate a valid reset of the device. However, the time to return from reset depends on what the device was doing at the time RP# went low.

2.3.1 RP# GOING LOW IN READ MODES

If RP# goes low when the device is in the read array, read identifier, or read status modes (with no program or erase operation in progress), then the device will reset and enter deep power-down mode for as long as RP# is held low. The minimum time that RP# must stay low to produce a valid reset is specified by t_{PLPH}. In this case, the part will be ready to read (write) after a delay t_{PHQV} (t_{PHWL} or t_{PHEL}) from when RP# goes high (Fig. 1A)

2.3.2 RP# GOING LOW DURING A PROGRAM OR ERASE

If RP# goes low when a program or erase operation is in progress, Smart 5 boot block products require a delay to shut down the in-progress operation. During this time, the device is unavailable for reads or writes. In contrast, the SmartVoltage product will reset regardless what mode (read, program, erase) it is in when RP# goes low.

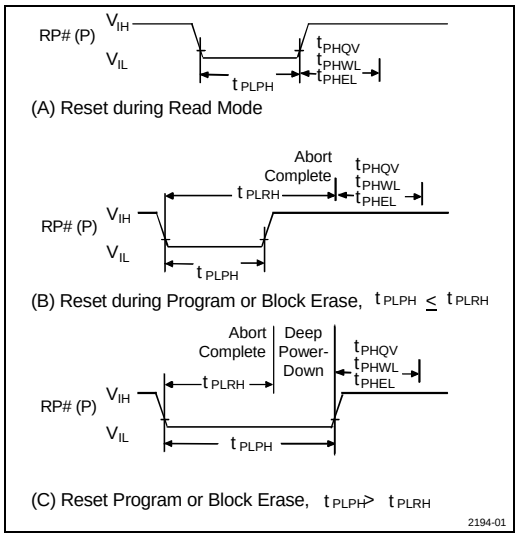

Figure 1. Reset Timing Waveforms

If RP# is taken low for time t_{PLPH} during a program or erase operation, the operation will be aborted, invalidating the contents at the aborted byte/word (for program) or block (for erase). The abort process goes as follows: When RP# goes low, the device shuts down the operation in progress, a process which takes time t_{PLRH} to complete. After this time, t_{PLRH}, the part will either reset to read array mode (if RP# has gone high during t_{PLRH}, Fig. 1B) or enter deep power-down mode (if RP# is still logic low after t_{PLRH}, Fig. 1C). In both cases, after returning from an aborted operation, the relevant time t_{PHQV} (for reads) or t_{PHWL}/t_{PHEL} (for writes) must be waited before an operation can be initiated. These delays are referenced to the end of t_{PLRH} rather than when RP# goes high.

Since this difference exists only when the system resets the flash during program or erase, designs that tie RP# to V_{CC} will not encounter this timing. However, designs that either actively control RP# or connect it to a system reset will need to account for the t_{PLRH} timing. If the RP# signal is actively controlled, then the system must wait t_{PLRH} plus t_{PHQV} (or t_{PHWL}/t_{PHEL}) before accessing the part after resetting during a program or erase. Consider also the possibility that a system reset signal could reset both the flash and the CPU during a program or erase, in which case the flash would be unavailable to read for time $t_{PLRH} + t_{PHQV}$. If this is longer than the time for the CPU to come out of reset, a RC delay circuit can be inserted between the system reset signal and the CPU, so that the flash has time to reset properly.

APPENDIX A
SmartVoltage/SMART 5 PRODUCT CORRESPONDENCE

SmartVoltage		Smart 5		
Part Name	**Description**	**Part Name**	**Description**	**Notes**
E28F002BV	2-M, Commercial Temp, 40-TSOP	E28F200B5	2-M, Commercial Temp, 48-TSOP	1, 2, 3
E28F200CV	2-M, Commercial Temp, 48-TSOP			1, 2
E28F200BV	2-M, Commercial Temp, 56-TSOP			1, 2, 4
PA28F200BV	2-M, Commercial Temp, 44-PSOP	PA28F200B5	2-M, Comm Temp, 44-PSOP	1, 2
TE28F002BV	2-M, Extended Temp, 40-TSOP	E28F200B5	2-M, Extended Temp, 48-TSOP	1, 2, 3
TE28F200CV	2-M, Extended Temp, 48-TSOP			1, 2
TE28F200BV	2-M, Extended Temp, 56-TSOP			1, 2, 4
TB28F200BV	2-M, Extended Temp, 44-PSOP	TB28F200B5	2-M, Ext. Temp, 44-PSOP	1, 2
E28F004BV	4-M, Commercial Temp, 40-TSOP	E28F400B5	4-M, Commercial Temp, 48-TSOP	1, 2, 3
E28F400CV	4-M, Commercial Temp, 48-TSOP			1, 2
E28F400BV	4-M, Commercial Temp, 56-TSOP			1, 2, 4
PA28F400BV	4-M, Commercial Temp, 44-PSOP	PA28F400B5	4-M, Comm Temp, 44-PSOP	1, 2
TE28F004BV	4-M, Extended Temp, 40-TSOP	E28F400B5	4-M, Extended Temp, 48-TSOP	1, 2, 3
TE28F400CV	4-M, Extended Temp, 48-TSOP			1, 2
TE28F400BV	4-M, Extended Temp, 56-TSOP			1, 2, 4
TB28F400BV	4-M, Extended Temp, 44-PSOP	TB28F400B5	4-M, Ext. Temp, 44-PSOP	1, 2
E28F008BV	8-M, Commercial Temp, 40-TSOP	E28F800B5	8-M, Commercial Temp, 48-TSOP	1, 2, 3
E28F800CV	8-M, Commercial Temp, 48-TSOP			1, 2
E28F800BV	8-M, Commercial Temp, 56-TSOP			1, 2, 4
PA28F800BV	8-M, Commercial Temp, 44-PSOP	PA28F800B5	8-M, Comm Temp, 44-PSOP	1, 2
TE28F008BV	8-M, Extended Temp, 40-TSOP	E28F800B5	8-M, Extended Temp, 48-TSOP	1, 2, 3
TE28F800CV	8-M, Extended Temp, 48-TSOP			1, 2
TE28F800BV	8-M, Extended Temp, 56-TSOP			1, 2, 4
TB28F800BV	8-M, Extended Temp, 44-PSOP	TB28F800B5	8-M, Ext. Temp, 44-PSOP	1, 2

NOTES:

1. All products are available in Top and Bottom boot versions.
2. SmartVoltage part access times are supported by the corresponding Smart 5 part, except for the -120 speed, which is not available on Smart 5 products. Smart 5 commercial temperature products support -60 ns and -80 ns for 2-M and 4-M densities; -70 ns and -90 ns for 8 M. Smart 5 extended temperature products support -80 ns for 2-M and 4-M densities; -90 ns for 8 M.
3. Smart 5 boot block products are not available in the 40-TSOP package; use the Smart 5 48-TSOP in x8 mode instead.
4. Smart 5 boot block products are not available in the 56-TSOP package; use the Smart 5 48-TSOP in x16 mode instead.

APPENDIX B
ADDITIONAL INFORMATION(1,2)

Order Number	Document
292154	*2/4/8-Mbit SmartVoltage Boot Block Flash Memory Family Overview*
290599	*Smart 5 Boot Block Flash Memory Family Datasheet*
290531	*2-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet*
290530	*4-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet*
290539	*8-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet*

NOTE:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.