AP-623

APPLICATION NOTE

Multi-Site Layout Planning with Intel's Boot Block Flash Memory

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1.0 INTRODUCTION

Flash memory has become an integral part of today's design environment. It spans a gamut of applications, from industrial products to household items. Flash memory can be found in point-of-sale terminals and barcode scanners; closer to home, flash memory is an important part of many cellular phones as well as personal computers. With so many uses, it is no wonder flash memory comes in so many different flavors and sizes.

With so many choices available on the market today, design engineers are placed in the precarious position of having to choose the best technological fit for their application while maintaining enough flexibility to permit real-time changes to accommodate market requirements. For example, the pinout and package offerings from one manufacturer may not necessarily be compatible with those of another.

This application note provides a means for designers to build in flexibility without sacrificing technology or exposing themselves to undue risk. This application note focuses on compatible layouts between Intel's Boot Block products (for upgrading from one density or package to another) as well as layouts that support multiple vendors flash memory offerings. This is not meant to be an exhaustive list by any means; rather it is intended as an illustration of how careful planning during the design stages of a product can provide additional flexibility at critical junctures when changes are required. All the layouts cited in this document are available on Intel's bulletin board system (BBS) and World Wide Web page.

2.0 INTEL'S BOOT BLOCK FLASH MEMORY

Due to the vast array of uses flash memory encompasses, it is difficult to cover the entire scope of flexible layout strategies for all available flash memory. Instead, this application note focuses on a subset of this large picture: Boot Block flash memory. Boot Block flash memory is an asymmetrically-blocked architecture (see Figure 1) that ranges in density from 1- Mbit (128K x 8) to 8-Mbit (1024K x 8 or 512K x 16). The individually-lockable boot block, which can be thought of as a ROM, is intended for storage of critical code segments. The two parameter blocks may be used to store code or data segments previously placed in E^2 devices. The main block(s) are available for mass storage of code and/or data. The tri-function capability of Boot Block flash memory is a large part of its appeal. It is widely used in PC applications to safeguard the BIOS, the basic input/output system without which the PC will not function.

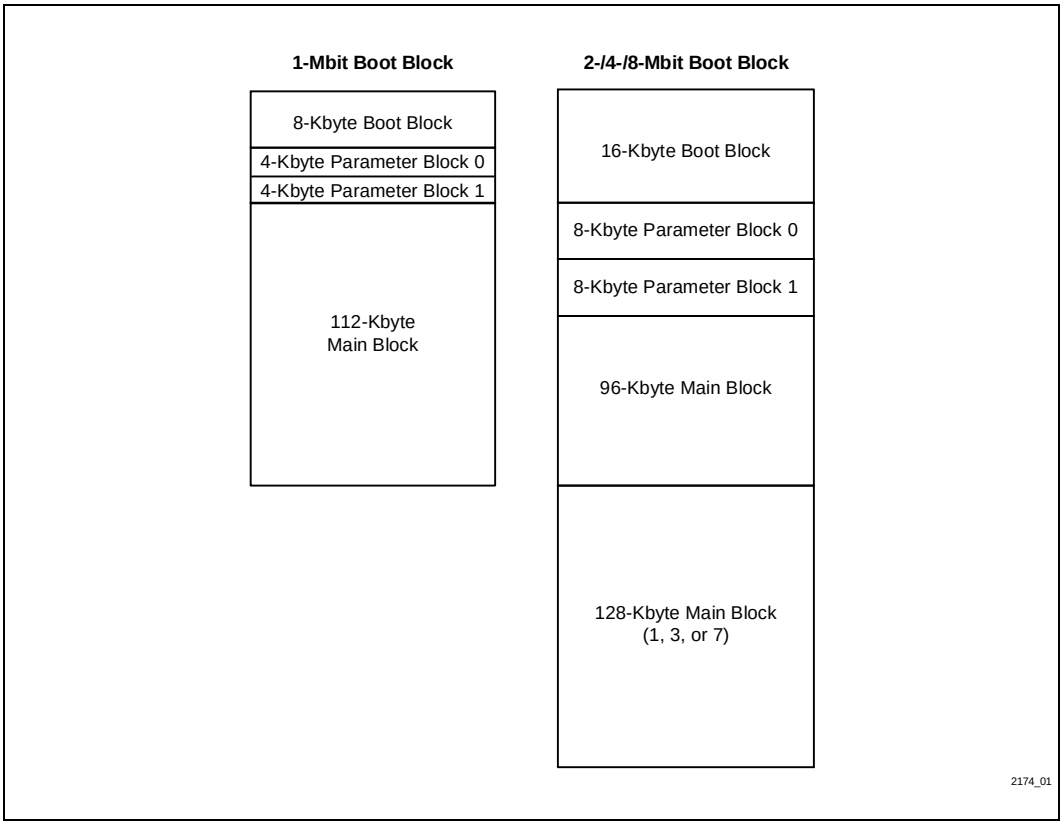


Figure 1. Intel Boot Block Flash Memory Architecture

3.0 BOOT BLOCK PACKAGE AND PINOUT OPTIONS

As mentioned earlier, flash memory products come in many flavors and sizes. Boot Block flash is no exception. Intel's Boot Block flash memory is available in x8 only or x8/x16 configurations. The 1-Mbit Boot Block flash memory is available in a 32-pin J-leaded chip carrier (PLCC), a 32-pin plastic dual in-line package (PDIP), and a 32-lead thin small outline package (TSOP). The 1-Mbit density is only available in x8 configuration, regardless of package.

The 2-Mbit, 4-Mbit, and 8-Mbit Boot Block products are offered in 40-lead, 48-lead, and 56-lead TSOP or 44-lead plastic small outline package (PSOP, sometimes referred to as SOP). The 40-lead TSOP package is x8 only. The 48-lead and 56-lead TSOP devices are x8/x16 configurable. The PSOP package can be configured to operate in either x8 or x16 mode using the BYTE# input pin (see Figure 2). The pinout of the 8-Mbit device is identical to that of the 4-Mbit device; the pinout of a 4-Mbit device is pin-compatible with that of a 2-Mbit device. This enables easy upgrades from one density to another.

It is clearly apparent the choice of package has a direct correlation to the flexibility of a design. Previously, PLCC and PDIP packages dominated the market. As probers, steppers, and handlers advanced in capability, new packages were developed to enable smaller form factors. Additionally, space requirements grew more stringent, making it necessary to combine the features of several devices into one package, thereby decreasing board space requirements.

Today, a TSOP package is the smallest form factor available. It has a 0.500 mm (20 Mils) lead pitch and maximum height of 1.2 mm (47 Mils). The 40-lead package has a nominal width of 10.0 mm (394 Mils) and length, including leads, of 20.0 mm (787 Mils). A PSOP package, in comparison, has 1.27 mm (50 Mils) lead pitch, which is the same as a PLCC package. The maximum height of a PSOP is 2.95 mm (116 Mils); the package dimensions are 16.0 mm (630 Mils) by 28.3 mm (1,110 Mils). Bear in mind the numbers provided above are package dimensions. When laying out a board that will accommodate differing packages, landpad measurements must be used. Landpad dimensions are slightly larger than package dimensions to accommodate offsets in package placement.

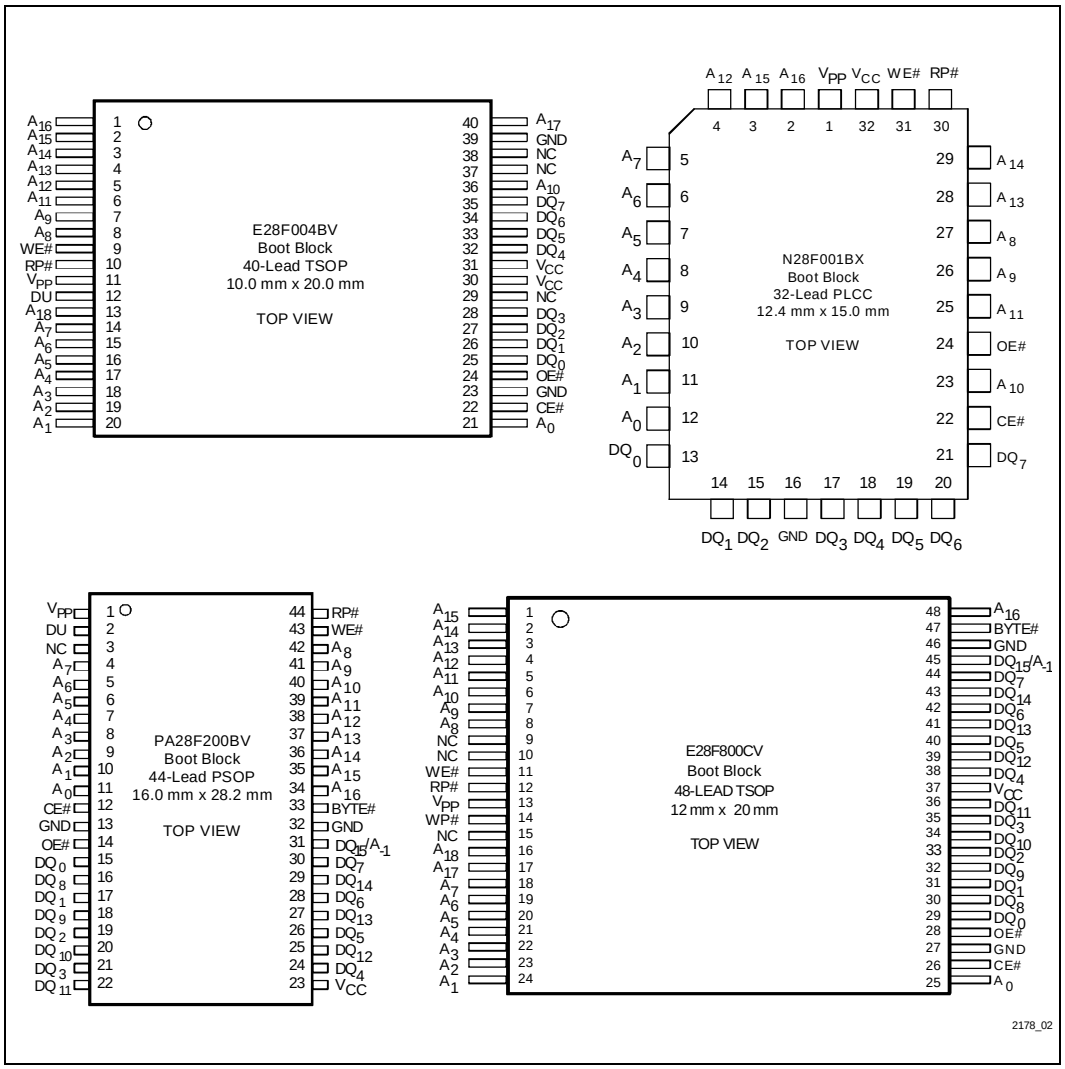


Figure 2. Example Boot Block Packages and Pinouts

Table 1. PCB Layout Descriptions

Case	Section
Intel 1-Mb Boot Block (32-L PLCC) to Intel 2-Mb Boot Block (44-L PSOP)	4.1.1
Intel 1-Mb Boot Block (32-L PLCC) to Intel 2-Mb Boot Block (40-L TSOP)	4.1.2
Intel 1-Mb Boot Block (32-L TSOP) to Intel 2-Mb Boot Block (40-L TSOP)	4.1.3
Intel 1-Mb Boot Block (32-L PDIP) to Intel 2-Mb Boot Block (44-L PSOP)	4.1.4
Intel 1-Mb Boot Block (32-L PDIP) to Intel 2-Mb Boot Block (40-L TSOP)	4.1.5
AMD 29F040 Symmetrically-Blocked Flash (32-L PLCC) to Intel 4-Mb Boot Block (44-L PSOP)	4.2.1
AMD 29F040 Symmetrically-Blocked Flash (32-L PLCC) to Intel 4-Mb Boot Block (40-L TSOP)	4.2.1
AMD 29F040 Symmetrically-Blocked Flash (32-L TSOP) to Intel 4-Mb Boot Block (40-L TSOP)	4.2.1
Atmel 29C040 Symmetrically-Blocked Flash (40-L TSOP) to Intel 4-Mb Boot Block (40-L TSOP)	4.2.2

4.0 BOOT BLOCK PCB LAYOUTS

The high-density layouts contained in this document were generated using Intel's small form factor design rules. All layouts presented in this application note assume a four-layer stack: signal-power-ground-signal. The section on board design considerations looks at other possible layer stacks and their advantages and disadvantages. Since power and ground pins are generally connected to their respective planes, V_{CC} and GND pins have been left unconnected. In addition, other pins requiring higher voltage (12V V_{PP} for instance) have also been left unconnected. The traces for these inputs are usually isolated from standard traces (to reduce crosstalk). They also tend to be shorter (to limit transmission line effects) than standard signal traces.

Layouts were designed using the PADS 2000* layout package, available from PADS Software, Inc. The Gerber outputs generated are industry-standard and can be used on any PCB layout tool that accepts the Gerber input format. Postscript files are also available. These can be printed on any postscript printer (in the event a layout tool is not readily accessible). Table 1 provides a complete list of Boot Block layouts referenced in this application note.

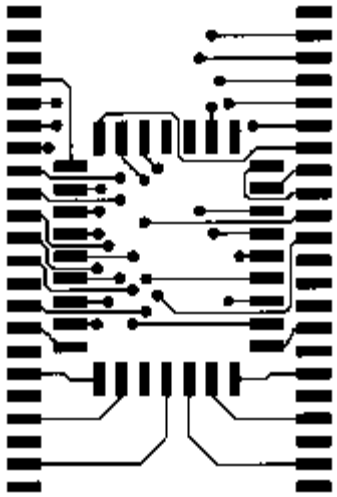
4.1 Intel 1-Mbit Boot Block to 2-Mbit Boot Block

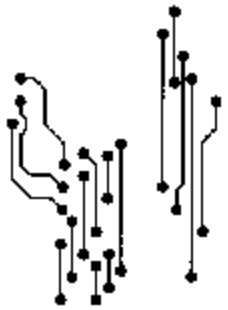
Most BIOS applications today utilize the 1-Mb Boot Block flash memory device. However, the wall is rapidly being reached as integration techniques continue to pack more into a system. BIOS engineers have been compressing code in order to fit the growing system BIOS requirements within the allotted 128 Kbyte available memory space. The emergence of Plug and Play and Universal Serial Bus will undoubtedly push BIOS code over the 1-Mb limit. The layouts in this section provide flexibility between 1-Mb and 2-Mb densities.

4.1.1 32-LEAD PLCC TO 44-LEAD PSOP

The layout in Figure 3 shows a 32-L PLCC (1-Mb flash) to a 44-L PSOP (2-Mb flash) memory. Both the PLCC and the PSOP have 50 Mil lead pitch, making them more rugged and easier to handle manually. As the layout shows, the PLCC can be placed entirely within the PSOP, thus minimizing the space consumption. Connecting address lines 17 and 18 on the PSOP package provides an upgrade path from 1 Mbit to 4 Mbit or 8 Mbit. The parameters used to derive this layout are given in the following table.

Feature	Dimension
Total Layout Area (PLCC to PSOP)	0.800” sq. (515.50 mm^2)
X,Y	0.730 “ x 1.096” (18.53 mm x 27.82 mm)
Via Size	0.025” (0.635 mm)
Trace Width	0.005” (0.127 mm)
Trace-to-Trace Clearance	0.006” (0.152 mm)
Trace-to-Pad Clearance	0.006” (0.152 mm)
Pad-to-Pad Clearance	0.008” (0.203 mm)





LAYER 1 **LAYER 2**

2178_03

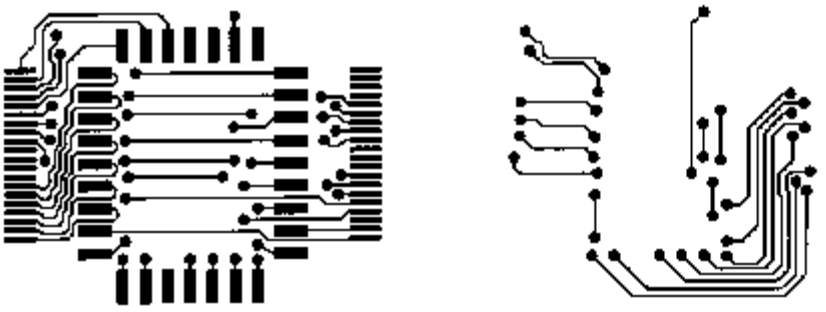
NOTE:
Scale = 3:1

Figure 3. 1-Mbit Boot Block (32-Lead PLCC) to 2-Mbit Boot Block (44-Lead PSOP)

4.1.2 32-LEAD PLCC TO 40-LEAD TSOP

For truly space-constrained designs, a TSOP package is the best choice. Although the 20 Mil lead pitch of the TSOP are smaller than those of the PLCC, that same smaller lead pitch makes the TSOP package ideal for notebook applications. A desktop system can also take advantage of the a TSOP package to reduce space requirements, which will reduce the overall system cost. As shown in Figure 4, a 40-lead TSOP package takes up almost the same amount of space as a PLCC package. The parameters used to derive this layout are given in the table below.

Feature	Dimension
Total Layout Area (PLCC to TSOP)	0.558" sq. (359.29 mm^2)
X,Y	0.845 " x 0.660" (21.45 mm x 16.75 mm)
Via Size	0.025" (0.635 mm)
Trace Width	0.005" (0.127 mm)
Trace-to-Trace Clearance	0.006" (0.152 mm)
Trace-to-Pad Clearance	0.006" (0.152 mm)
Pad-to-Pad Clearance	0.006" (0.152 mm)



LAYER 1 **LAYER 2**

2178_04

NOTE:
Scale = 3:1

Figure 4. 1-Mbit Boot Block (32-Lead PLCC) to 2-Mbit Boot Block (40-Lead TSOP)

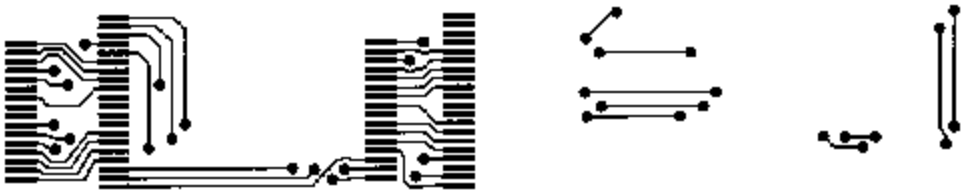
PLCC Layouts and Bulk Flash Memory

It is important to note that both 32-L PLCC layouts can be used for Intel's 1-Mb and 2-Mb Bulk flash devices. Both the Boot Block 1-Mb and the 1-Mb/2-Mb Bulk flash memory have identical pinouts in the PLCC package, with the exception of pin 30. This pin is a no connect on the bulk devices, but is used as the RP# pin on the Boot Block devices. In the above layouts, pin 30 is unconnected.

4.1.3 32-LEAD TSOP TO 40-LEAD TSOP

For designs using the 1-Mb Boot Block in the 32-lead TSOP package, the upgrade path of choice is to the 40-lead TSOP 2-Mb flash memory. With a slight shift in the placement, as illustrated in Figure 5, a minimal footprint can be obtained that enables both devices to be interchanged on any given board. This kind of flexibility protects your design during constrained times and also allows multiple sources at your discretion. The parameters used to derive this layout are given in the table below.

Feature	Dimension
Total Layout Area (PLCC to PSOP)	0.800" sq. (277.46 mm^2)
X,Y	1.053 " x 0.409" (26.73 mm x 10.38 mm)
Via Size	0.025" (0.635 mm)
Trace Width	0.005" (0.127 mm)
Trace-to-Trace Clearance	0.006" (0.152 mm)
Trace-to-Pad Clearance	0.006" (0.152 mm)
Pad-to-Pad Clearance	0.006" (0.152 mm)

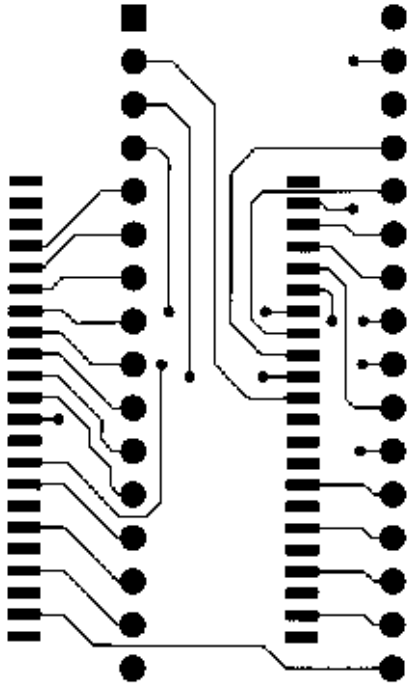


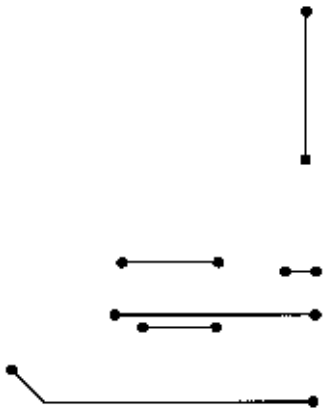
NOTE:
Scale = 3:1

Figure 5. 1-Mbit Boot Block (32-Lead TSOP) to 2-Mbit Boot Block (40-Lead TSOP)

4.1.4 32-LEAD PDIP TO 44-LEAD PSOP

Customers using the PDIP package are usually not concerned about space. Although this package may be durable, especially for manual handling, it is being replaced by the PSOP and TSOP packages. The layout for converting a PDIP to a PSOP is given in Figure 6.





LAYER 1 **LAYER 2**

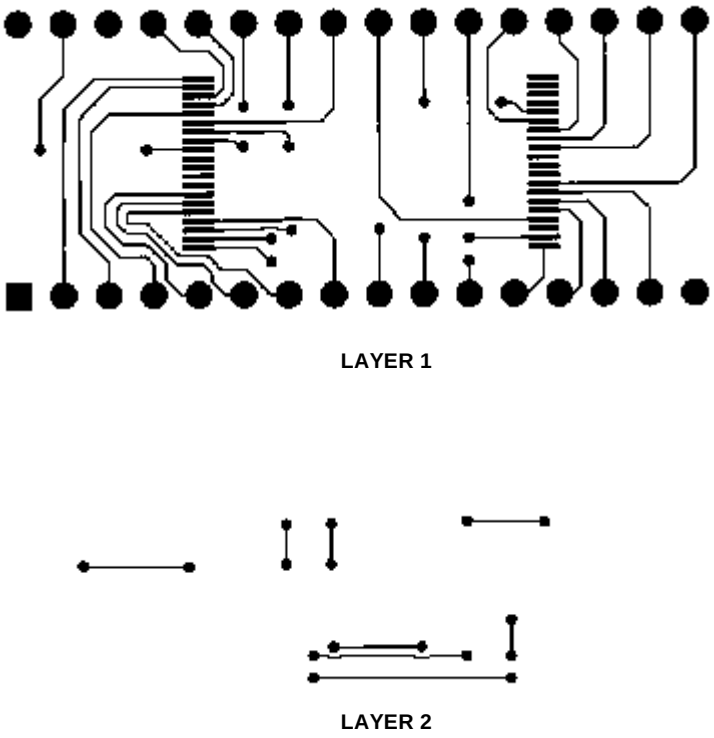
2178_06

NOTE:
Scale = 3:1

Figure 6. 1-Mbit Boot Block (32-Lead PDIP) to 2-Mbit Boot Block (44-Lead PSOP)

4.1.5 32-LEAD PDIP TO 40-LEAD TSOP

The layout for converting a PDIP to a TSOP is shown in Figure 7. Notice the tremendous space savings accomplished with this shift in package. This layout supports upgrading from a 1-Mbit boot block to a 2-Mb, 4-Mb, or 8-Mb Boot Block flash memory.



NOTE:
Scale = 3:1

Figure 7. 1-Mbit Boot Block (32-Lead PDIP) to 2-Mbit Boot Block (40-Lead TSOP)

4.2 Other Flash Memories to Intel Boot Block Flash Memory

The really unique aspect of multi-site layouts is the ability to support multiple vendors on the same board. By placing dual footprints on a board, a design can be made to support, say, both an Intel 4-Mb flash device and an AMD 4-Mb flash device. There may be some software changes required, but the flexibility realized outweighs the software inconvenience. Additionally, software changes tend to be less costly than complete board redesign for new package types.

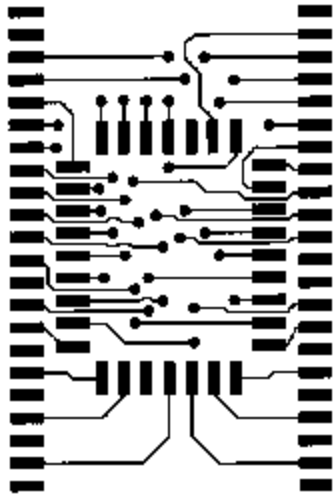
As market changes take place, customer needs will drive peaks and valleys on the supply and demand curve. During surplus supply situations, multi-site layouts may not be of much benefit, but their value during constrained supply times cannot be refuted. With dual footprints on a board, a design can utilize multiple vendor products, thus making it more adaptable to the changing times yet to come.

4.2.1 AMD 4-MBIT SYMMETRICALLY-BLOCKED FLASH TO INTEL 4-MBIT BOOT BLOCK FLASH

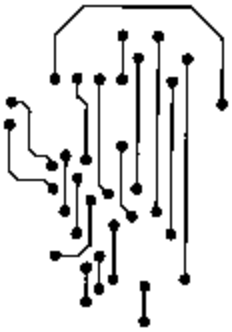
AMD's 4-Mb sector erase flash memory contains eight, equal-sized 64-KB blocks. For designs that use this device, software emulation techniques will allow the same design to use both the Intel 4-Mb Boot Block flash memory and AMD's 4-Mb Sector Erase flash memory. The actual algorithms that accomplish this are not covered in this application note; however, the dual package footprint that describes the hardware layout is discussed in this section.

For designs using the 32-lead PLCC, Figure 8 depicts the diagram for the PLCC package to the 44-lead PSOP package. The PLCC to 40-lead TSOP layout is shown in Figure 9. The parameters that correspond to each layout are listed in the tables preceding each layout drawing. Although the diagrams look similar to previous ones, the actual routing of the traces is different due to different pin assignments across different manufacturers' products.

Feature	Dimension
Total Layout Area (PLCC to PSOP)	0.800" sq. (515.50 mm^2)
X,Y	0.730 " x 1.096" (18.53 mm x 27.82 mm)
Via Size	0.025" (0.635 mm)
Trace Width	0.005" (0.127 mm)
Trace-to-Trace Clearance	0.006" (0.152 mm)
Trace-to-Pad Clearance	0.006" (0.152 mm)
Pad-to-Pad Clearance	0.008" (0.203 mm)



LAYER 1



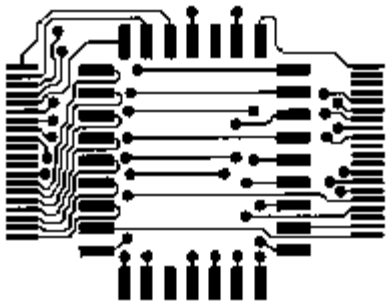
LAYER 2

2178_08

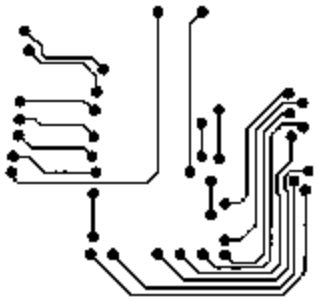
NOTE:
Scale = 3:1

Figure 8. AMD 4-Mbit Sector Erase (32-Lead PLCC) to Intel 4-Mbit Boot Block (44-Lead PSOP)

Feature	Dimension
Total Layout Area (PLCC to TSOP)	0.558” sq. (359.29 mm^2)
X,Y	0.845 “ x 0.660” (21.45 mm x 16.75 mm)
Via Size	0.025” (0.635 mm)
Trace Width	0.005” (0.127 mm)
Trace-to-Trace Clearance	0.006” (0.152 mm)
Trace-to-Pad Clearance	0.006” (0.152 mm)
Pad-to-Pad Clearance	0.006” (0.152 mm)



LAYER 1



LAYER 2

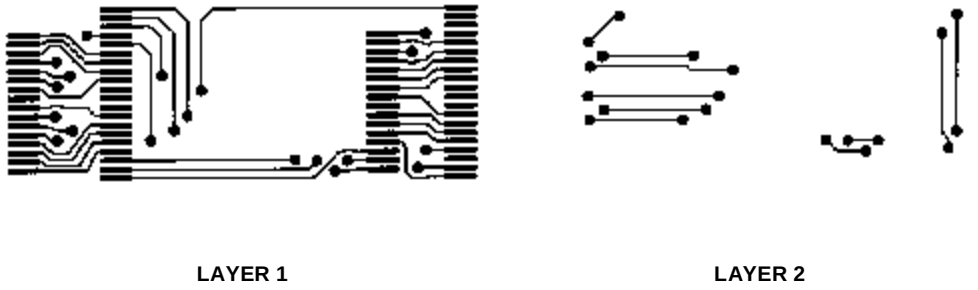
2178_09

NOTE:
Scale = 3:1

Figure 9. AMD 4-Mbit Sector Erase (32-Lead PLCC) to Intel 4-Mbit Boot Block (40-Lead TSOP)

The AMD 29F040 is also available in a 32-lead TSOP package. If a particular design uses this package and desires the features of a Boot Block device, the diagram in Figure 10 shows how a board can be laid out such that it supports both TSOP pinouts. The parameters used to derive this layout are given in the table below.

Feature	Dimension
Total Layout Area (TSOP to TSOP)	0.431” sq. (277.46 mm^2)
X,Y	1.053 “ x 0.409” (26.73 mm x 10.38 mm)
Via Size	0.025” (0.635 mm)
Trace Width	0.005” (0.127 mm)
Trace-to-Trace Clearance	0.006” (0.152 mm)
Trace-to-Pad Clearance	0.006” (0.152 mm)
Pad-to-Pad Clearance	0.006” (0.152 mm)



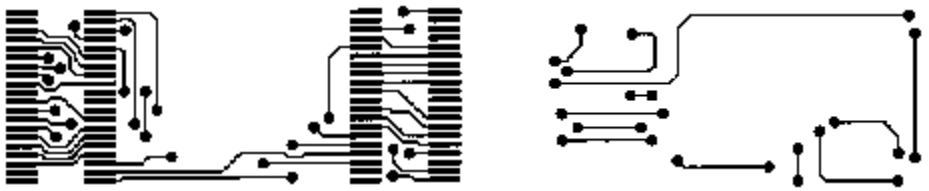
NOTE:
Scale = 3:1

Figure 10. AMD 4-Mbit Sector Erase (32-Lead TSOP) to Intel 4-Mbit Boot Block (40-Lead TSOP)

4.2.2 ATMEL 4-MBIT CMOS FLASH TO INTEL 4-MBIT BOOT BLOCK FLASH

Atmel also produces a 4-Mb symmetrically-blocked flash memory. However, they do not offer it in a PLCC package. It is available only in a 32-lead plastic DIP or a 40-lead TSOP package. The blocking of the two devices is also different: the Atmel device has 1024 equally-sized blocks of 512 bytes each. Again, software emulation schemes (which are not discussed in this document) can be employed to make one device mimic the functionality of the other. Therefore, the same board can be populated by either device, depending on market requirements. The layout in Figure 11 shows how a 40-lead TSOP footprint of the AT29C040 can co-exist on the same board as an Intel 4-Mb Boot Block flash memory. Again, note that even though the diagram looks somewhat similar to previous layouts, this layout depicts two 40-lead devices with different pinouts. The parameters used to derive this layout are given in the table below.

Feature	Dimension
Total Layout Area (TSOP to TSOP)	
X,Y	
Via Size	0.025” (0.635 mm)
Trace Width	0.005” (0.127 mm)
Trace-to-Trace Clearance	0.006” (0.152 mm)
Trace-to-Pad Clearance	0.006” (0.152 mm)
Pad-to-Pad Clearance	0.006” (0.152 mm)



LAYER 1 **LAYER 2**

2178_11

NOTE:
Scale = 3:1

Figure 11. Atmel 4-Mbit Sector Erase (40-Lead TSOP) to Intel 4-Mbit Boot Block (40-Lead TSOP)

5.0 PRINTED CIRCUIT BOARD (PCB) DESIGN CONSIDERATIONS

PCB design is one of the most critical aspects of a system. It is the medium through which signals will propagate from one component to another. The board is the electrical backbone of any design. If logic levels are slightly off, they can be tweaked to perfection; however, if the inherent electrical characteristics are incorrect, no amount of tweaking will improve the design in the long term. Therefore, care should be taken to insure that board design is not only functional but also forward-looking, in anticipation of potential problem areas.

5.1 Power and Ground Planes

Power and ground planes should be designed first. The design of these planes depends on signal rise time (by far the most important), the number of signals, the physical dimensions of the board, and estimated trace widths. Power and ground planes should be placed together to maximize capacitive coupling and reduce power supply noise. Additional ground planes may be used to isolate signal routing layers; however, to guard against warping effects, power and/or ground planes should be used in pairs.

It is common knowledge that current follows the paths of least resistance. However, at high frequencies current follows the path of least inductance. This is relevant because the path of least inductance for board traces is under the conductor of the transmitted signal, as shown in Figure 12. Board designers can insure return current flow as close to the transmitted signal as possible by using many ground vias to connect ground planes together. With a mixture of power and ground planes, current has a tendency to flow through many bypass capacitors. This, unfortunately, introduces radiated noise into the system.

In high-speed designs, crosstalk can exist in the ground plane. Crosstalk between two conductors depends on their mutual inductance and mutual capacitance. Inductive crosstalk is usually larger than capacitive crosstalk in a digital environment. Returning signal current (which are traveling on the same ground plane for the most part), generate magnetic fields. These magnetic fields induce noise voltages proportional to the rate of change of the driving signal into all circuit elements in their path. Short rise time generate larger voltage as a result of mutual inductance. Slotted ground planes exacerbate the problem by forcing currents to flow together around the slot (since return signal currents cannot flow through the slot). This has the effect of increasing signal length, and therefore, mutual inductance.

5.2 Trace Considerations

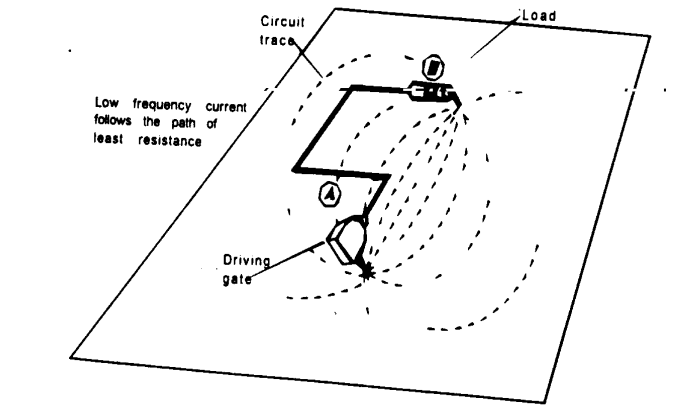
Today's motherboards are stacked designs, consisting of as little as two layers to as much as eight or ten layers. When routing traces on the board, double tracking (two traces between adjacent pins) should be avoided. Additionally, triple- and four-track routing is also not a good idea. This practice can cause severe crosstalk problems. Although system designers tend to use fewer traces to minimize costs, this usually results in tightly-packed traces. Tightly-spaced traces have more crosstalk and have power handling capability. Depending on the design, tradeoffs may be necessary to accommodate system requirements.

5.3 Package Effects

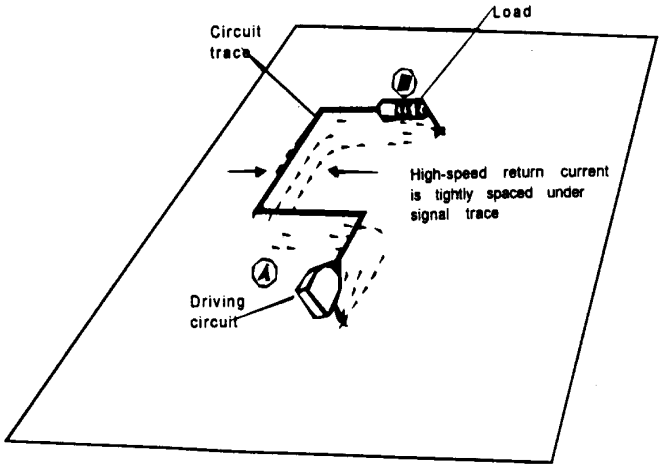
Nearly all packages encounter problems at high speeds. Package lead inductance, lead capacitance, and heat dissipation are at the root of the problem. Individual pins on a package can cause the phenomenon known as ground bounce due to lead inductance of ground pins. This ground bounce is localized to the device and perceived as an internal glitch on the input signals because of the variance in the ground reference. Calculating the ground bounce magnitude necessitates knowing the rise time, lead inductance, load capacitance, and switching voltage. Of course, consideration must be given to whether the board operates at TTL or CMOS levels.

Package lead capacitance produces a slightly different effect from lead inductance. Stray capacitance between the adjacent pins of a component couples noise onto sensitive input pins. This problem grows worse with faster rise times and higher input impedance connections.

Increased heat dissipation through a package is a common side effect of most high-speed designs. As one might expect, different packages behave to temperature differently. For most logic devices, however, the relationship between temperature and power is linear. The internal temperature of a package, referred to as the junction temperature, is a function of the ambient temperature and thermal resistance. Thermal resistance is a property of cooling attachments (e.g., fans, heat sinks, etc.), package size, package material, and die attach method.



Low Frequency Current Path (Least Resistance)



High Frequency Current Path (Least Inductance)

2178_12

Figure 12. Current at High Frequencies Follows the Path of Least Inductance

6.0 CONCLUSION

The name of the game, in life as well as in business, is change: if you want to play, you have to learn to adapt. It is no mystery market needs will change: demographics will shift, purchasing trends will meander from one side to the other, and buying habits will bounce up and down like the stock market. To be successful, your designs need to be flexible.

Designing for flexibility means being able to adapt to changes as they happen, not after it is too late. Flexibility needs to be designed into the product at the beginning not after it has already hit the market. The techniques presented in this application note make it easier for your application to adapt. By designing-in multiple footprints (especially if it is within the same space as previously consumed by the component), eliminates headaches when another of life's little surprises springs up. Dual footprints can make all the difference, especially when demand outpaces supply and alternative solutions become the norm.

As a final note, a design should have as much flexibility built-in as possible. If you are not space-constrained and can handle multiple package layouts in your application, an investigation of the benefit of multi-site layouts is a good idea. The layouts presented in this application note are all two package diagrams. More layers will be needed as the number of packages supported increases. Since four layer boards are common, laying out a board that can support two or three different package types is not only possible but an excellent answer to a constantly changing environment. Change may be the only constant, but preparation minimizes its effects.

7.0 ADDITIONAL INFORMATION

7.1 References

Order Number	Document
290531	2-Mbit (128K X 16, 256K X 8)Smart Voltage Boot Block FlashFile™ Memory Family Datasheet
290530	4-Mbit (256K X 16, 512K x 8) SmartVoltage Boot Block FlashFile™ Memory Family Datasheet
290539	8-Mbit (512K X 16, 1M X 8) SmartVoltage Boot Block FlashFile™ Memory Family Datasheet
292159	AP-607, "Multi-Site Layout Planning with Intel's FlashFile™ Components, Including ROM Capability"
292130	AB-57, "Intel's Flash memory Boot Block Architecture for Safe Firmware Updates"
292154	AB-60, "2/4/8-Mbit SmartVoltage Boot Block Flash Memory Family Overview"

7.2 Revision History

Number	Description
-001	Original version
-002	Added previously omitted PDIP layouts; made textual corrections