AP-611

APPLICATION NOTE

Boot Block Compatibility: 2/4-Mbit BX/BL with 2/4/8-Mbit BV

PETER HAZEN
SENIOR TECHNICAL MARKETING ENGINEER

COLLIN K. ONG
TECHNICAL MARKETING ENGINEER

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1.0 INTRODUCTION

This application note describes compatibility between 12V V_{PP} 2-Mbit and 4-Mbit boot block flash memories (BX/BL) manufactured on Intel's 0.8 µ ETOX™ III process and the complete 2-, 4- and 8-Mbit family of SmartVoltage boot block flash memories (BV) manufactured on Intel's 0.6 µ ETOX™ IV process. While software is compatible between the two families, several simple hardware design steps are necessary to enable a single socket or board site to accept both BX/BL boot block and SmartVoltage boot block components. Differences in DC and AC characteristics for all operational and temperature ranges should also be taken into account during system design.

The conversion checklist below will assist in the conversion process of existing BX/BL designs to SmartVoltage BV products.

Table 1. 4-Step Program for Converting BX/BL Designs to BV

Step	Action
1	Determine BV product name associated with the BX or BL product (see Table 2)
2	Account for pinout differences between BX/BL and BV a. See pinouts, Figures 1 – 4 b. Account for WP# pin (Sections 3.1, 3.6)
3	Account for DC and AC characteristic differences (Section 3.3, 3.4, Appendix A)
4	Check other differences mentioned in this document and BV errata document

2.0 SOFTWARE COMPATIBILITY

2.1 Bus Operations, Commands and Device/Manufacturer IDs

Both the BX/BL products and the BV SmartVoltage boot block products share the same command definitions and bus operations. The device/manufacturer IDs are also identical, allowing full software compatibility.

2.2 Status Register

Status Register definition is the same for both families of products with the exception of bit 3 which indicates V_{PP} Status. The 12V boot block products only allow successful program and erase operations at 12V V_{PP}. The V_{PP} Status bit will indicate a low-V_{PP} condition for these products if V_{PP} drops below V_{PPL} (max), specified at 6.5V. For SmartVoltage products, however, program and erase is supported at 5V V_{PP}, so the V_{PP} Status bit indicates a low-V_{PP} condition only if V_{PP} drops below V_{PPLK}, specified at 1.5V.

3.0 HARDWARE COMPATIBILITY

3.1 Packages and Pinouts

Figures 1, 2, and 3 illustrate the pinout differences for the 40-ld TSOP, 44-ld PSOP and 56-ld TSOP packages at the 4-Mbit density. Key differences in pinout definitions include the following:

- The "Don't Use" (DU) pin on the BX/BL products is replaced by the WP# pin on the SmartVoltage boot block products on each pinout. Since SmartVoltage products allow program and erase operations with V_{PP} at 5V as well as 12V, the WP# pin was added to provide a way to lock or unlock the boot block in-system with 5V instead of the 12V required for the BX/BL products. Refer to Section 3.6 of this application note for a complete description of this pin.

- The BX/BL products require at 12V V_{PP} for successful program and erase operations. When V_{PP} is switched below V_{PPL} = 6.5V, the entire flash memory is protected against accidental program or erase commands. Since the SmartVoltage products allow program and erase at 5V V_{PP} in addition to 12V, the V_{PP} pin must be switched to V_{PPLK} = 1.5V, to implement program and erase protection on the entire flash memory.

3.2 Density Upgrade Path

The SmartVoltage boot block family offers an upgrade path of 2-, 4-, and 8-Mbits in the 40-ld TSOP, 44-ld PSOP and 48-ld TSOP packages shown in Appendix C. Upgrading BX/BL designs to BV makes this path available for future code storage needs.

The 48-ld TSOP package (Figure 4) is new for the SmartVoltage boot block products, as it is not offered for the BX/BL boot block components. The 8-Mbit component is not offered in the 56-ld package. Note that WP# functionality is not provided for the 44-ld PSOP version of the 8 Mbit. See Section 3.7 for more information.

Table 2. Product Name Comparison

Density	Organization	12V Boot Block (BX) Products (V_{CC} = 5V)	12V Boot Block (BL) Products (V_{CC} = 3.3V)	SmartVoltage Boot Block (BV) Products
2 Mbit	128 Kbytes x16, or 256 Kbytes x8	28F200BX	28F200BL	28F200BV 28F200CV
	256 Kbytes x8	28F002BX	28F002BL	28F002BV
4 Mbit	256 Kbytes x16, or 512 Kbytes x8	28F400BX	28F400BL	28F400BV 28F400CV
	512 Kbytes x8	28F004BX	28F004BL	28F004BV
8 Mbit	512 Kbytes x16, or 1024 Kbytes x8	N/A	N/A	28F800BV 28F800CV
	1024 Kbytes x8	N/A	N/A	28F008BV

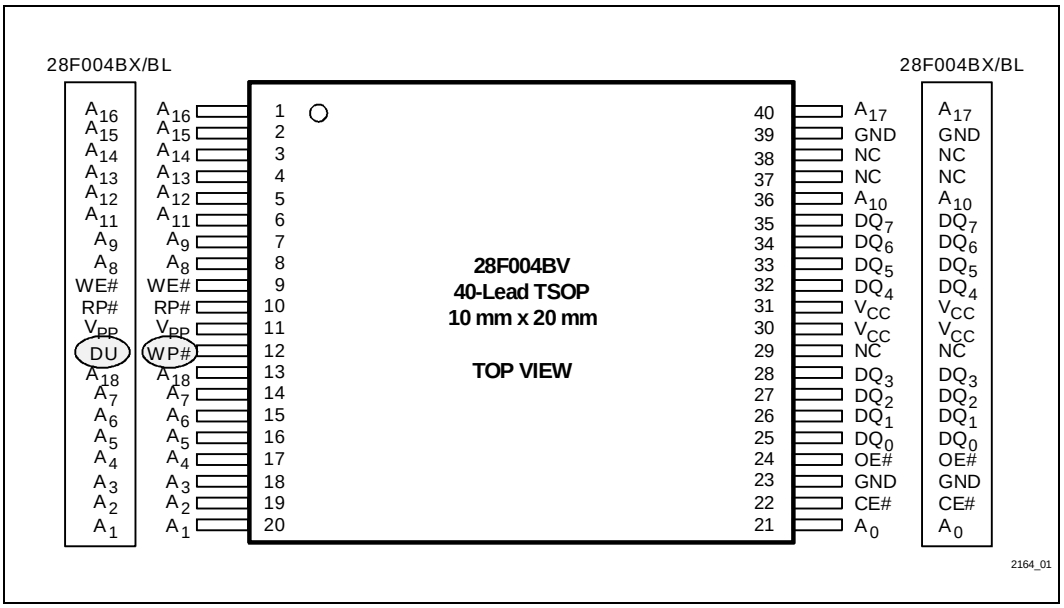


Figure 1. 40-Lead TSOP Compatibility (Available at 2-, 4- and 8-Mbit Densities)

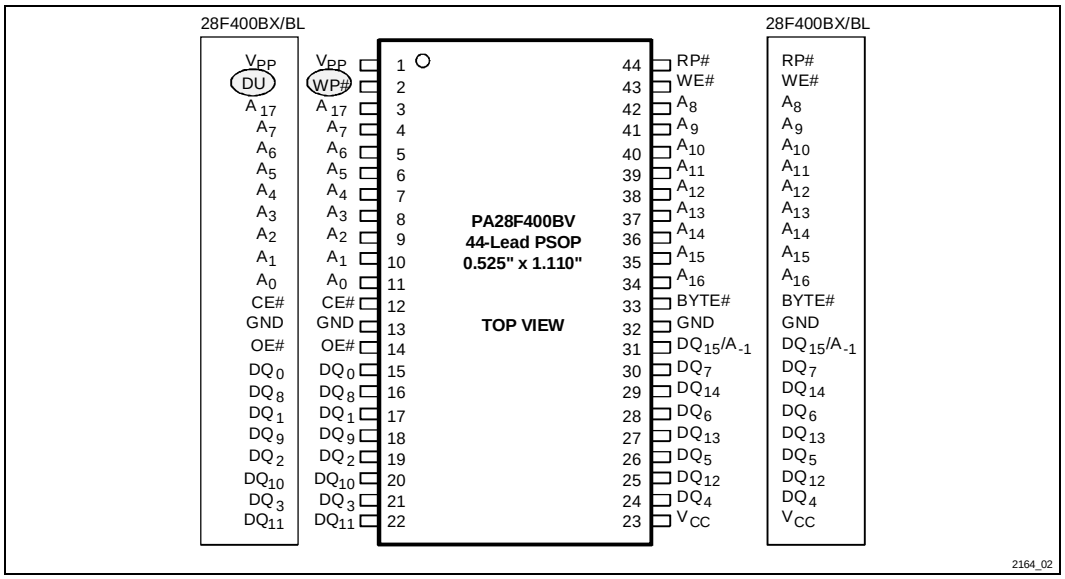


Figure 2. 44-Lead PSOP Compatibility (Available at 2-, 4- and 8-Mbit Densities)

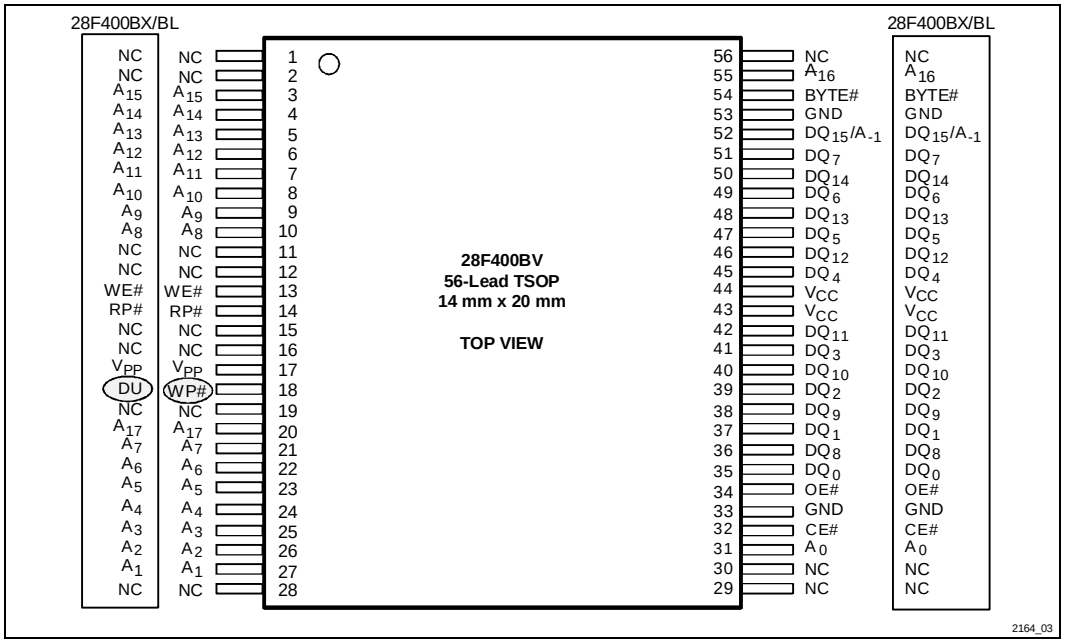


Figure 3. 56-Lead TSOP Compatibility (Available at 2- and 4-Mbit Densities)

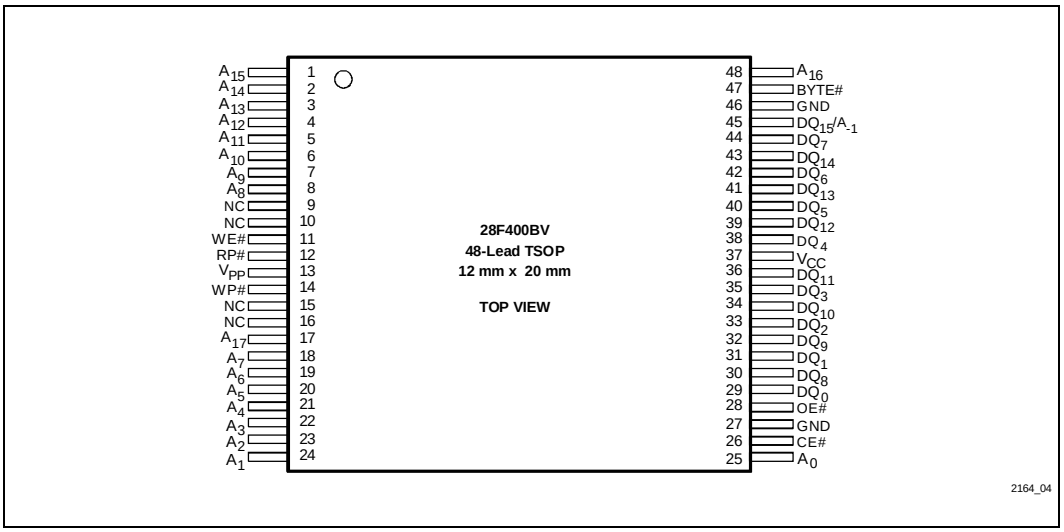


Figure 4. New 48-Lead TSOP Package for the 2/4/8-Mbit SmartVoltage Boot Block Products

3.3 Specification Changes for SmartVoltage Products

While the BX/BL boot block components and SmartVoltage BV boot block components contain similar functionality, there are some differences due to the use of different circuit designs and process technologies.

Table 3 provides an index to spec comparisons in Appendix A that contain specifications that have changed between the two the BX/BL and BV products.

The following two sections attempt to characterize the changes. These guidelines cannot replace careful appraisal of the impact of particular spec differences on a design. The errata/addendum document should also be checked for any other design issues.

3.3.1 DC CHARACTERISTICS

Generalizing over the various voltage and temperature ranges, the current draw specs can be characterized as:

1. Read, standby, and power-down I_{CC} currents for the BV SmartVoltage products are about 10% higher.
2. Write and erase currents (I_{CC} and I_{PP}) for BV SmartVoltage products are from 10–50% lower.
3. Identifier (V_{ID}) and RP# unlock voltage range (V_{HH}) has changed from 11.5–13.0V (BX/BL) to 11.4–12.6V on BV SmartVoltage products.
4. The maximum "safe" voltage for V_{PP} (where the device contents are protected from alteration) has changed from V_{PPL} = 6.5V (BX/BL) to V_{PPLK} = 1.5V (BV) due to the addition of 5V write/erase capability.

3.3.2 AC CHARACTERISTICS

Most AC timing specs are identical or better when moving from BX/BL products to BV SmartVoltage products. The differences can be characterized as follows:

1. Some reset timing specs, such as t_{PHQV}, t_{PHWL}, and t_{PHEL}, are significantly longer on SmartVoltage BV products than on BX/BL products.
2. When comparing 3.3V V_{CC} operation, the expanded temperature BL (–20°C to +70°C) is compared to extended temperature BV (–40°C to +85°C). Due to the different operating ranges and circuit designs, a number of timing specs are different.
3. Some new specs that were not specified on BX/BL products, t_{PLPH} and t_{PLQZ} for example, have been added to the BV products. Reference the errata/addendum document for details.

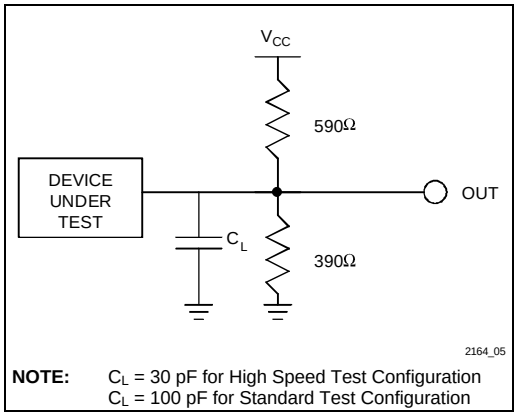
Check the appropriate table in Appendix A to determine precise spec differences.

Table 3. Index to Spec Comparisons in Appendix A

Table	Spec Type	Voltage Range	Temp Range
5	DC Characteristics (BX vs. BV)	5V ± 10%	Commercial
6	DC Characteristics (BX vs. BV)	5V ± 10%	Extended
7	DC Characteristics (BL vs. TBV)	3.3 ± 0.3V	BL Expanded vs. BV Extended
8	AC Characteristics: Read Operations (BX–60 vs. BV–60)	5V ± 5%	Commercial
9	AC Characteristics: Read Ops (BX–80/120 vs. BV–80/120)	5V ± 10%	Commercial
10	AC Characteristics: Read Ops (TBX–80 vs. TBV–80)	5V ± 10%	Extended
11	AC Characteristics: Read Ops (BL–150 vs. TBV–80)	3.3 ± 0.3V	BL Expanded vs. BV Extended
12	AC Characteristics: Write Ops (BX–60 vs. BV–60)	5V ± 5%	Commercial
13	AC Characteristics: Write Ops (BX–80/120 vs. BV–80/120)	5V ± 10%	Commercial
14	AC Characteristics: Write Ops (TBX–80 vs. TBV–80)	5V ± 10%	Extended
15	AC Characteristics: Write Ops (BL–150 vs. TBV–80)	3.3 ± 0.3V	BL Expanded vs. BV Extended

3.4 Test Load Configuration

The BV SmartVoltage parts are tested using a different test load setup that the BX/BL use. Figure 5 shows the BV's testing configuration. Since all of the device specifications are tested using this test load, the impact of this change on system timing should be checked to ensure smooth upgrades.



NOTE: C_L = 30 pF for High Speed Test Configuration
C_L = 100 pF for Standard Test Configuration

Figure 5. BV SmartVoltage Test Configuration

3.5 V_{CC} Switching/Ramp-Up

SmartVoltage BV specifications include a delay between the time V_{CC} reaches the minimum of its voltage range and the time RP# can go high, releasing the part from reset into normal operation. This delay is required by the BV product's SmartVoltage circuitry to detect which voltage range, 3.3V or 5V, is being provided.

Table 4. V_{CC} Supply Switching/Ramp-Up Timing

Sym	Parameter	Min	Unit
t_{5VPH}	V_{CC} at 4.5 (min) to RP# High	2	µs
t_{3VPH}	V_{CC} at 3.0 (min) to RP# High	2	µs

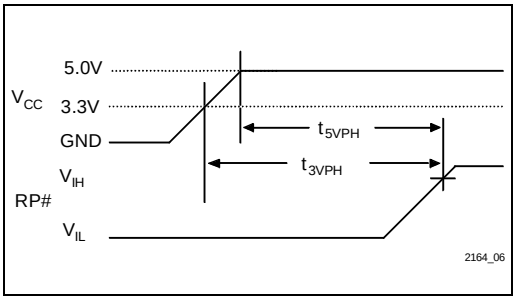


Figure 6. V_{CC} Supply Switching/Ramp-Up

3.6 V_{PP} Voltage Ranges

The SmartVoltage technology used in the BV product gives it the capability to program and erase using either 12V ± 5% or 5V ± 10% on the V_{PP} pin. The BX product offers a 12V ± 10% V_{PP} option, which reduces cycling to 100 erase cycles. The BV products do not support this V_{PP} mode, even at reduced cycling.

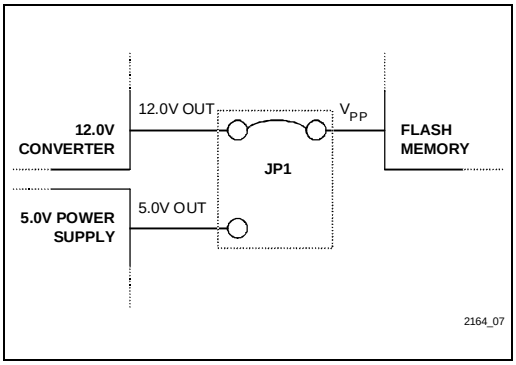


Figure 7. Flexible V_{PP} Voltage Setup

3.6.1 WRITE PROTECTION WITH V_{PPLK}

Since boot block products do not support locking for blocks other than the boot block, one method of implementing write protection for the rest of the flash array is to take V_{PP} below V_{PPLK} (previously called V_{PPL} for BX/BL). When V_{PP} is below V_{PPLK}, any commands, such as program or erase, that would modify data in the flash array will return a error in the status register. For BX/BL products, V_{PPLK} (V_{PPL}) was specified at 6.5V (max). However, since SmartVoltage BV parts allow program and erase with V_{PP} at 5V, V_{PPLK} has been lowered on BV products to 1.5V (max).

Designs lowering V_{PP} below 6.5V for write protection should now lower V_{PP} below 1.5V to ensure that both BX/BL and BV components are write protected.

3.7 WP# Pin for Write Protection

The BV SmartVoltage products include a new input pin, WP#, which was not on BX/BL pinouts. The WP# pin replaces the DU (Don't Use) pin on BX/BL pinouts and provides a method for controlling the locking of the boot block with a logic-level signal.

The WP# input on BV pinouts must be driven and not left floating. On BX/BL designs, the DU pin can be driven to voltages between GND and V_{CC}, for purposes of BV compatibility. The WP# (DU on BX/BL) pin should be driven to logic high or low, or tied to a control signal to allow dynamic locking/unlocking on SmartVoltage parts, as shown in Figure 8.

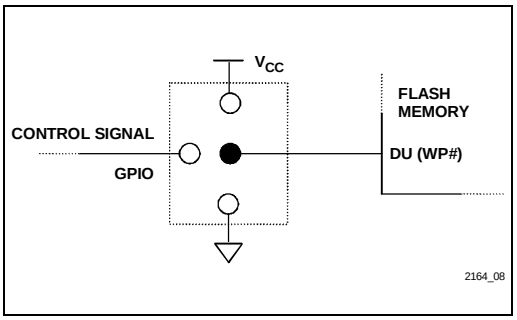


Figure 8. Enabling "DU" Pin Upgrade to WP#

In order to make the BV part function like the BX/BL parts, the WP# pin should be tied to ground. If this is done, boot block locking will be controlled by the RP# pin in the same manner as on BX/BL products. Table 5 details the control signals for write protecting the SmartVoltage flash component.

For the 8-Mbit 44-ld PSOP product version, the WP# pin has been replaced by the highest order address due to pin count constraints. In this package and density, boot block unlocking is controlled by RP# only, operating as if WP# is internally tied to logic low.

Table 5. Write Protection Controls

V_{PP}	RP#	WP#	Write Protection
V_{IL}	X	X	All Blocks Locked
≥ V_{PPLK}	V_{IL}	X	All Blocks Locked (Reset)
≥ V_{PPLK}	V_{HH}	X	All Blocks Unlocked
≥ V_{PPLK}	V_{IH}	V_{IL}	Boot Block Locked
≥ V_{PPLK}	V_{IH}	V_{IH}	All Blocks Unlocked

4.0 ADDITIONAL INFORMATION

4.1 References

Order Number	Document
292154	AB-60 “2/4/8-Mbit SmartVoltage Boot Block Flash Memory Family”
290448	28F200BX-T/B, 28F002BX-T/B 2-Mbit (128K x 16, 256K x 8) Boot Block Flash Memory Family Datasheet
290451	28F400BX-T/B, 28F004BX-T/B 4-Mbit (256K x 16, 512K x 8) Boot Block Flash Memory Family Datasheet
290449	28F200BX-TL/BL, 28F002BX-TL/BL 2-Mbit (128K x 16, 256K x 8) Low Power Boot Block Flash Memory Family Datasheet
490450	28F400BX-TL/BL, 28F004BX-TL/BL 4-Mbit (256K x 16, 512K x 8) Low Power Boot Block Flash Memory Family Datasheet
290531	2-Mbit (128K x 16, 256K x 8) SmartVoltage Boot Block Flash Memory Datasheet
290530	4-Mbit (256K x 16, 512K x 8) SmartVoltage Boot Block Flash Memory Datasheet
290539	8-Mbit (512K x 16, 1M x 8) SmartVoltage Boot Block Flash Memory Family Datasheet
297595	Errata/Addendum Information for 4-Mbit Boot Block SmartVoltage Flash Memories
297612	Errata/Addendum Information for 2-Mbit Boot Block SmartVoltage Flash Memories
297187	Errata/Addendum 2/4-Mbit Boot Block Flash Memory
FaxBack* 2294	“2/4/8-Mbit SmartVoltage Technical Support Summary”

FaxBack information available at 1-800-628-2283 or (916) 356-3105

4.2 Revision History

Number	Description
-001	Original version

APPENDIX A
AC AND DC CHARACTERISTICS TABLES

NOTE

Please refer to the respective product datasheet table notes for specific parameter information.

Table 6. SmartVoltage 4-Mb Added/Revised DC Characteristics (Commercial)

Sym	Parameter	BX–60 BX–80 BX–120			BV–60 BV–80 BV–120			Units	Test Conditions
		V_{CC} = 5V ± 10%							
		Min	Typ	Max	Min	Typ	Max		
I_{CCS}	V_{CC} Standby Current			1.5		0.8	2.0	mA	V_{CC} = V_{CC} Max CE# = RP# = BYTE# = WP# = V_{IH}
				100		50	130	µA	V_{CC} = V_{CC} Max CE# = RP# = V_{CC} ± 0.2V
I_{CCD}	V_{CC} Deep Power-Down Current		0.2	1.2		0.2	8	µA	V_{CC} = V_{CC} Max V_{IN} = V_{CC} or GND RP# = GND ± 0.2V
I_{CCR}	V_{CC} Read Current for Word or Byte			55			60	mA	**CMOS INPUTS** V_{CC} = V_{CC} Max CE# = GND, OE# = V_{CC} f = 10 MHz, I_{OUT} = 0 mA Inputs = GND ± 0.2V or V_{CC} ± 0.2V
				60			65	mA	**TTL INPUTS** V_{CC} = V_{CC} Max CE# = V_{IL}, OE# = V_{IH} f = 10 MHz, I_{OUT} = 0 mA Inputs = V_{IL} or V_{IH}
I_{CCW}	V_{CC} Write Current for Word or Byte			N/A		30	50	mA	Word Write in Progress V_{PP} = $V_{PPH}1$ (at 5V)
				65		30	45	mA	Word Write in Progress V_{PP} = $V_{PPH}2$ (at 12V)
I_{CCE}	V_{CC} Erase Current			N/A		18	35	mA	Block Erase in Progress V_{PP} = $V_{PPH}1$ (at 5V)
				30		18	30	mA	Block Erase in Progress V_{PP} = $V_{PPH}2$ (at 12V)

Table 6. SmartVoltage 4-Mb Added/Revised DC Characteristics (Commercial) (Continued)

Sym	Parameter	BX–60 BX–80 BX–120			BV–60 BV–80 BV–120			Units	Test Conditions
		V_{CC} = 5V ± 10%							
		Min	Typ	Max	Min	Typ	Max		
I_{PPW}	V_{PP} Word Write Current			N/A		13	25	mA	$V_{PP} = V_{PPH}1$ (at 5V) Word Write in Progress
				40		8	20	mA	$V_{PP} = V_{PPH}2$ (at 12V) Word Write in Progress
	V_{PP} Byte Write Current			30		8	20	mA	$V_{PP} = V_{PPH}2$ (at 12V) Byte Write in Progress
I_{PPE}	V_{PP} Erase Current			N/A		10	20	mA	$V_{PP} = V_{PPH}1$ (at 5V) Block Erase in Progress
				30		5	15		$V_{PP} = V_{PPH}2$ (at 12V) Block Erase in Progress
V_{ID}	A_9 Intelligent Identifier Voltage	11.5		13.0	11.4		12.6	V	
V_{PPL}	V_{PP} during Normal Operations	0.0		6.5	N/A		N/A	V	Complete Write Protection (BX)
V_{PPLK}	V_{PP} Lock-Out Voltage	N/A		N/A	0.0		1.5	V	Complete Write Protection (BV)
V_{HH}	RP# Unlock Voltage	11.5		13.0	11.4		12.6	V	Boot Block Write/Erase

Table 7. SmartVoltage 4-Mb Added/Revised DC Characteristics (Extended)

Sym	Parameter	TBX–80			TBV–80			Units	Test Conditions
		V_{CC} = 5V ± 10%							
		Min	Typ	Max	Min	Typ	Max		
I_{CCS}	V_{CC} Standby Current			1.5		0.8	2.5	mA	V_{CC} = V_{CC} Max CE# = RP# = BYTE# = WP# = V_{IH}
				100		70	150	µA	V_{CC} = V_{CC} Max CE# = RP# = V_{CC} ± 0.2V
I_{CCD}	V_{CC} Deep Power-Down Current(1)		0.2	20		0.2	8	µA	V_{CC} = V_{CC} Max V_{IN} = V_{CC} or GND RP# = GND ± 0.2V
I_{CCR}	V_{CC} Read Current for Word or Byte			60			65	mA	**CMOS INPUTS** V_{CC} = V_{CC} Max CE# = GND, OE# = V_{CC} f = 10 MHz, I_{OUT} = 0 mA Inputs = GND ± 0.2V or V_{CC} ± 0.2V
				65			70	mA	**TTL INPUTS** V_{CC} = V_{CC} Max CE# = V_{IL}, OE# = V_{IH} f = 10 MHz, I_{OUT} = 0 mA Inputs = V_{IL} or V_{IH}
I_{CCW}	V_{CC} Word or Byte Write Current for			N/A		30	50	mA	Write in Progress V_{PP} = $V_{PPH}1$ (at 5V)
				70		30	45	mA	Write in Progress V_{PP} = $V_{PPH}2$ (at 12V)
I_{CCE}	V_{CC} Erase Current			N/A		22	45	mA	Block Erase in Progress V_{PP} = $V_{PPH}1$ (at 5V)
				40		18	40	mA	Block Erase in Progress V_{PP} = $V_{PPH}2$ (at 12V)
I_{CCES}	V_{CC} Erase Suspend Current		5	10		5	12	mA	CE# = V_{IH} Block Erase Suspend
I_{PPD}	V_{PP} Deep Power-Down Current			5.0		0.2	10	µA	RP# = GND ± 0.2V

Table 7. SmartVoltage 4-Mb Added/Revised DC Characteristics (Extended) (Continued)

Sym	Parameter	TBX–80			TBV–80			Units	Test Conditions
		V_{CC} = 5V ± 10%							
		Min	Typ	Max	Min	Typ	Max		
I_{PPW}	V_{PP} Word Write Current			N/A		13	30	mA	$V_{PP} = V_{PPH}1$ (at 5V) Word Write in Progress
				40		8	25	mA	$V_{PP} = V_{PPH}2$ (at 12V) Word Write in Progress
	V_{PP} Byte Write Current			30		8	25		$V_{PP} = V_{PPH}2$ (at 12V) Byte Write in Progress
I_{PPE}	V_{PP} Erase Current			N/A		15	25	mA	$V_{PP} = V_{PPH}1$ (at 5V) Block Erase in Progress
				30		10	20	mA	$V_{PP} = V_{PPH}2$ (at 12V) Block Erase in Progress
V_{ID}	A_9 Intelligent Identifier Voltage	11.5		13.0	11.4		12.6	V	
V_{PPL}	V_{PP} during Normal Operations	0.0		6.5	N/A		N/A	V	Complete Write Protection (BX)
V_{PPLK}	V_{PP} Lock-Out Voltage	N/A		N/A	0.0		1.5	V	Complete Write Protection (BV)
V_{HH}	RP# Unlock Voltage	11.5		13.0	11.4		12.6	V	Boot Block Write/Erase

NOTE:

1. As determined by errata document.

Table 8. SmartVoltage 4-Mb Added/Revised DC Characteristics 3.3V BL Expanded (–20°C to +70°C) vs. BV Extended (–40°C to +85°C)(1)

Sym	Parameter	BL–150 (–20°C to +70°C)			TBV–80 (–40°C to +85°C)			Units	Test Conditions
		V_{CC} = 3.3V ± 0.3V							
		Min	Typ	Max	Min	Typ	Max		
I_{CCS}	V_{CC} Standby Current		0.45	0.12		0.4	1.5	mA	V_{CC} = V_{CC} Max CE# = RP# = BYTE# = WP# = V_{IH}
			45	120		60	110	µA	V_{CC} = V_{CC} Max CE# = RP# = V_{CC} ± 0.2V
I_{CCD}	V_{CC} Deep Power-Down Current		0.2	1.2		0.2	8	µA	V_{CC} = V_{CC} Max V_{IN} = V_{CC} or GND RP# = GND ± 0.2V
I_{CCR}	V_{CC} Read Current for Word or Byte			25			30	mA	**CMOS INPUTS** V_{CC} = V_{CC} Max CE# = GND, OE# = V_{CC} f = 5 MHz, I_{OUT} = 0 mA Inputs = GND ± 0.2V or V_{CC} ± 0.2V
				25			30	mA	**TTL INPUTS** V_{CC} = V_{CC} Max CE# = V_{IL}, OE# = V_{IH} f = 5 MHz, I_{OUT} = 0 mA Inputs = V_{IL} or V_{IH}
I_{CCW}	V_{CC} Write Current for Word or Byte			N/A		13	30	mA	Write in Progress V_{PP} = $V_{PPH}1$ (at 5V)
				30		10	25	mA	Write in Progress V_{PP} = $V_{PPH}2$ (at 12V)
I_{CCE}	V_{CC} Erase Current			N/A		13	30	mA	Block Erase in Progress V_{PP} = $V_{PPH}1$ (at 5V)
				20		10	25	mA	Block Erase in Progress V_{PP} = $V_{PPH}2$ (at 12V)
I_{CCES}	V_{CC} Erase Suspend Current		3	6		3	8.0	mA	CE# = V_{IH} Block Erase Suspend
I_{PPD}	V_{PP} Deep Power-Down Current			5		0.2	10	µA	RP# = GND ± 0.2V

Table 8. SmartVoltage 4-Mb Added/Revised DC Characteristics 3.3V BL Expanded (–20°C to +70°C) vs. BV Extended (–40°C to +85°C)(1) (Continued)

Sym	Parameter	BL–150 (–20°C to +70°C)			TBV–80 (–40°C to +85°C)			Units	Test Conditions
		V_{CC} = 3.3V ± 0.3V							
		Min	Typ	Max	Min	Typ	Max		
I_{PPW}	V_{PP} Word Write Current			N/A		13	30	mA	V_{PP} = V_{PPH}1 (at 5V) Word Write in Progress
				40		8	25	mA	V_{PP} = V_{PPH}2 (at 12V) Word Write in Progress
	V_{PP} Byte Write Current			30		8	25	mA	V_{PP} = V_{PPH}2 (at 12V) Byte Write in Progress
I_{PPE}	V_{PP} Erase Current			N/A		13	30	mA	V_{PP} = V_{PPH}1 (at 5V) Block Erase in Progress
				30		8	25	mA	V_{PP} = V_{PPH}2 (at 12V) Block Erase in Progress
V_{ID}	A_9 Intelligent Identifier Voltage	11.5		13.0	11.4		12.6	V	
V_{PPL}	V_{PP} during Normal Operations	0.0		6.5	N/A		N/A	V	Complete Write Protection (BX)
V_{PPLK}	V_{PP} Lock-Out Voltage	N/A		N/A	0.0		1.5	V	Complete Write Protection (BV)
V_{HH}	RP# Unlock Voltage	11.5		13.0	11.4		12.6	V	Boot Block Write/Erase

NOTE:
1. BL only +20°C to +70°C, BV available 0°C to +70°C or –40°C to +85°C

Table 9. SmartVoltage 4-Mb Added/Revised AC Read Characteristics (Commercial)

Sym	Parameter		BX–60				BV–60				Units
		V_{CC}	5V ± 5%		5V ± 10%		5V ± 5%		5V ± 10%		
		Load	30 pF		100 pF		30 pF		100 pF		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PHQV}	RP# to Output Delay			300		300		450		450	ns

Table 10. SmartVoltage 4-Mb Added/Revised AC Read Characteristics (Commercial)

Sym	Parameter		BX–80		BV–80		BX–120		BV–120		Units
		V_{CC}	5V ± 10%								
		Load	100 pF								
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PHQV}	RP# to Output Delay			300		450		300		450	ns

Table 11. SmartVoltage 4-Mb Added/Revised AC Read Characteristics (Extended)

Sym	Parameter		TBX–80		TBV–80		Units
		V_{CC}	5V ± 10%				
		Load	100 pF				
			Min	Max	Min	Max	
t_{PHQV}	RP# to Output Delay			300		450	ns

Table 12. SmartVoltage 4-Mb Added/Revised AC Read Characteristics 3.3V BL Expanded (–20°C to +70°C) vs. BV Extended (–40°C to +85°C)(1)

Sym	Parameter		BL–150 (–20°C to 70°C)		TBV–80 (–40°C to 85C)		Units
		V_{CC}	3.3 ± 0.3V				
		Load	50 pF				
			Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time		150		110		ns
t_{AVQV}	Address to Output Delay			150		110	ns
t_{ELQV}	CE# to Output Delay			150		110	ns
t_{PHQV}	RP# to Output Delay			600		800	ns
t_{ELFL}/ t_{ELFH}	CE# Low to BYTE# High or Low			5		7	ns
t_{AVFL}	Address to BYTE# High or Low			5		7	ns
t_{FLQV}/ t_{FHQV}	BYTE# to Output Delay			150		110	ns

NOTE:

1. BL only +20°C to +70°C, BV available 0°C to +70°C or –40°C to +85°C

Table 13. SmartVoltage 4-Mb Added/Revised AC Write Characteristics 5V (Commercial)

Sym	Parameter		BX–60				BV–60				Units
		V_{CC}	5V ± 5%		5V ± 10%		5V ± 5%		5V ± 10%		
		Load	30 pF		100 pF		30 pF		100 pF		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PHWL}	RP# High Recovery to WE# Going Low		215		215		450		450		ns
t_{PHEL}	RP# High Recovery to CE# Going Low		215		215		450		450		ns

Table 14. SmartVoltage 4-Mb Added/Revised AC Write Characteristics 5V (Commercial)

Sym	Parameter		BX–80		BV–80		BX–120		BV–120		Units
		V_{CC}	5V ± 10%								
		Load	100 pF								
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PHWL}	RP# High Recovery to WE# Going Low		215		450		215		450		ns
t_{PHEL}	RP# High Recovery to CE# Going Low		215		450		215		450		ns

Table 15. SmartVoltage 4-Mb Added/Revised AC Write Characteristics (Extended)

Sym	Parameter		TBX–80		TBV–80		Units
		V_{CC}	5V ± 10%				
		Load	100 pF				
			Min	Max	Min	Max	
t_{PHWL}	RP# High Recovery to WE# Going Low		215		450		ns
t_{PHEL}	RP# High Recovery to CE# Going Low		215		450		ns

Table 16. SmartVoltage 4-Mb Added/Revised AC Write Characteristics 3.3V BL Expanded (–20°C to +70°C) vs. BV Extended (–40°C to +85°C)(1)

Symbol	Parameter		BL–150 (–20°C to +70°C)		TBV–80 (–40°C to +85°C		Units
		V_{CC}	3.3 ± 0.3V				
		Load	50 pF				
			Min	Max	Min	Max	
WE#-Controlled Writes							
t_{AVAV}	Write Cycle Time		150		110		ns
t_{PHWL}	RP# High Recovery to WE# Going Low		1000		800		ns
t_{AVWH}	Address Setup to WE# Going High		95		90		ns
t_{DVWH}	Data Setup to WE# Going High		100		90		ns
t_{WLWH}	WE# Pulse Width		100		90		ns
t_{WHEH}	CE# Hold from WE# High		10		0		ns
t_{WHWL}	WE# Pulse Width High		50		20		ns
CE#-Controlled Writes							
t_{AVAV}	Write Cycle Time		150		110		ns
t_{PHEL}	RP# High Recovery to CE# Going Low		1000		800		ns
t_{AVEH}	Address Setup to CE# Going High		95		90		ns
t_{DVEH}	Data Setup to CE# Going High		100		90		ns
t_{ELEH}	CE# Pulse Width		100		90		ns
t_{EHWH}	WE# Hold from CE# High		10		0		ns
t_{EHEL}	CE# Pulse Width High		50		20		ns

NOTE:

1. BL only +20°C to +70°C, BV available 0°C to +70°C or –40°C to +85°C

APPENDIX B
ORDERING INFORMATION

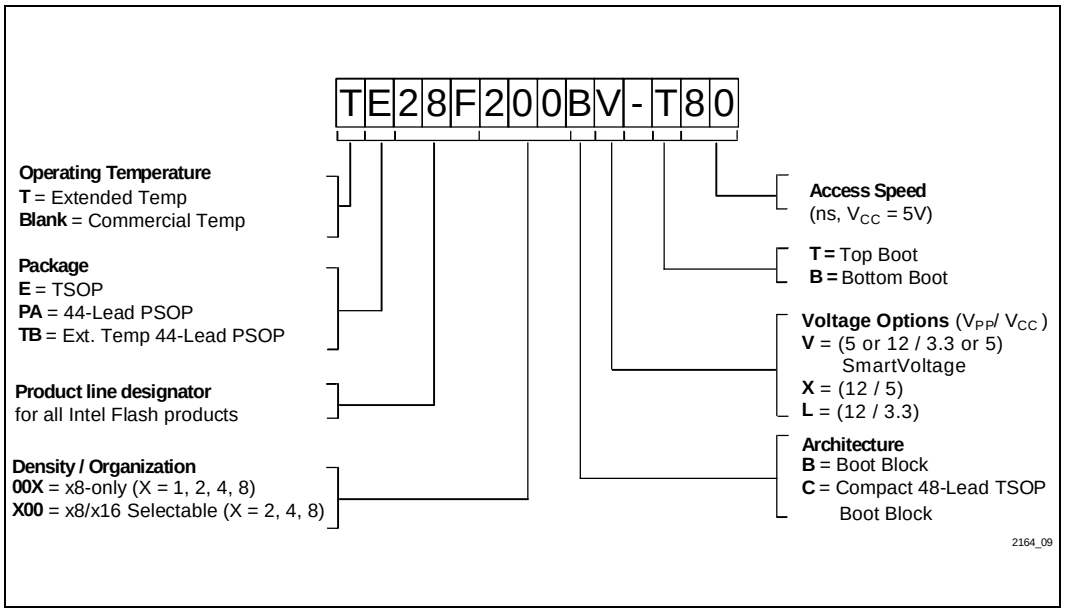


Figure 9. Decoding the Boot Block Product Names

APPENDIX C
SmartVoltage PACKAGE PINOUTS

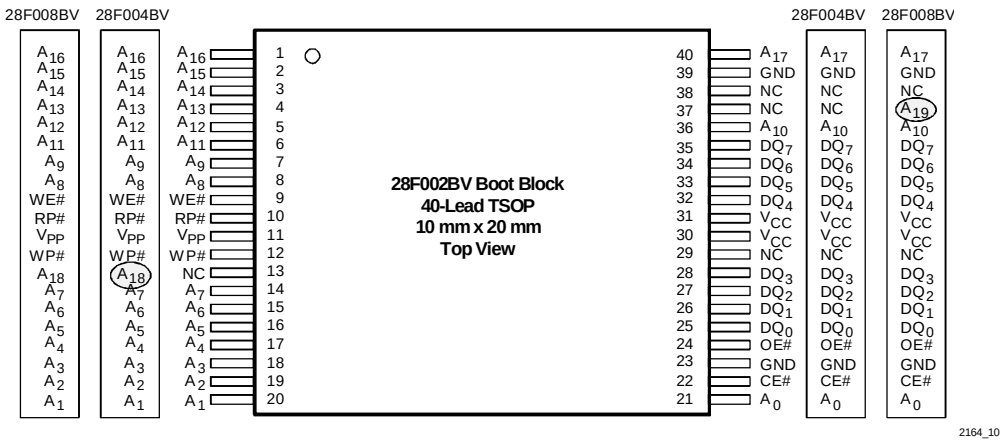
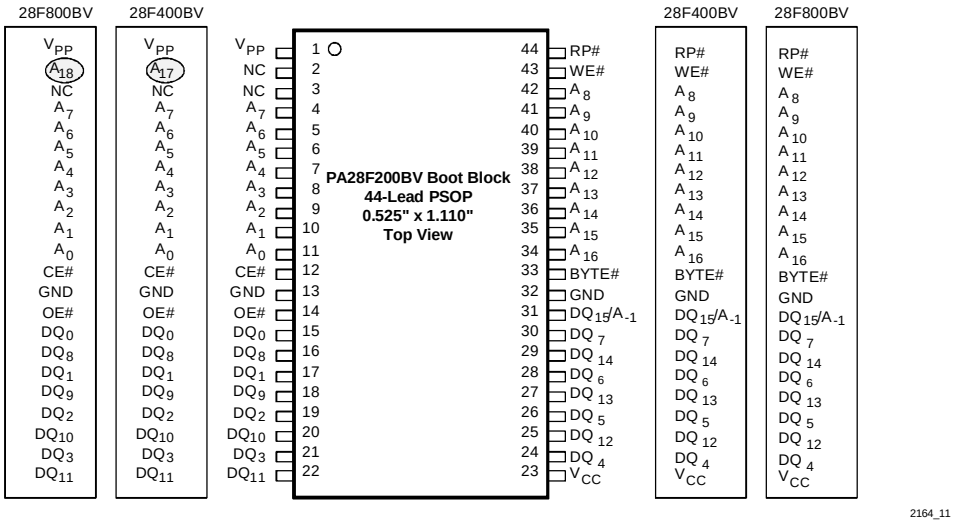


Figure 10. The 40-Lead TSOP Offers the Smallest Form Factor for Space-Constrained Applications



NOTE: Pin 2 is WP# on 2/4 Mbit (DU for BX/BL), but for the 8-Mbit BV device, pin 2 has been changed to A_{18}. Designs planning on upgrading to the 8-Mbit density from the 2/4-Mbit density in this package should design pin 2 to control WP# functionality at the 2/4-Mbit level and allow for pin 2 to control A_{18} after upgrading to the 8-Mbit density.

Figure 11. The 44-Lead PSOP Offers Convenient Upgrade from JEDEC ROM Standards

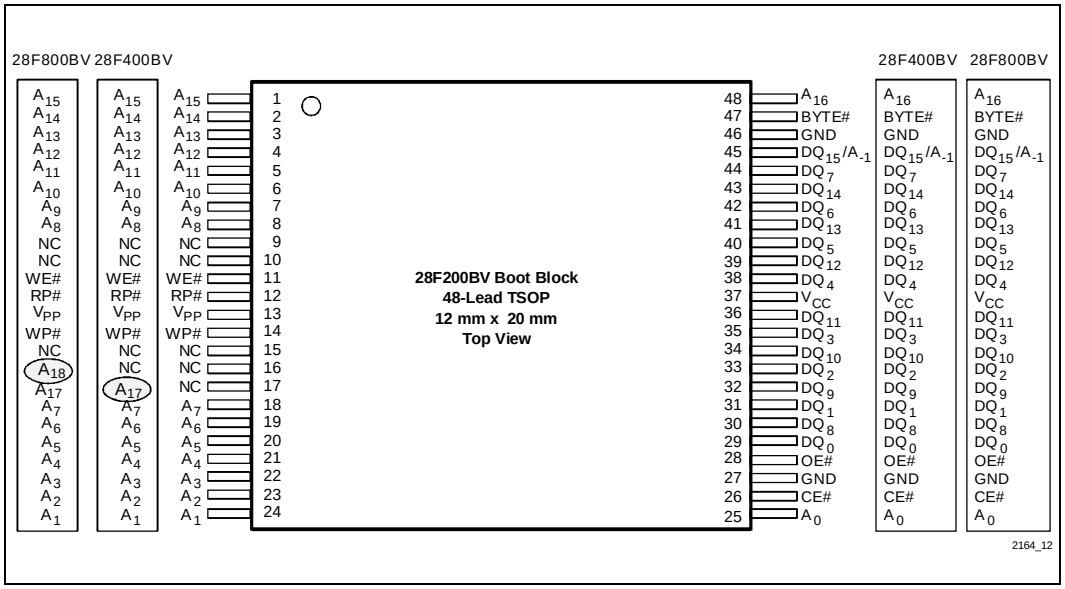


Figure 12. The 48-Lead TSOP Offers the Smallest Form Factor for x16 Operation

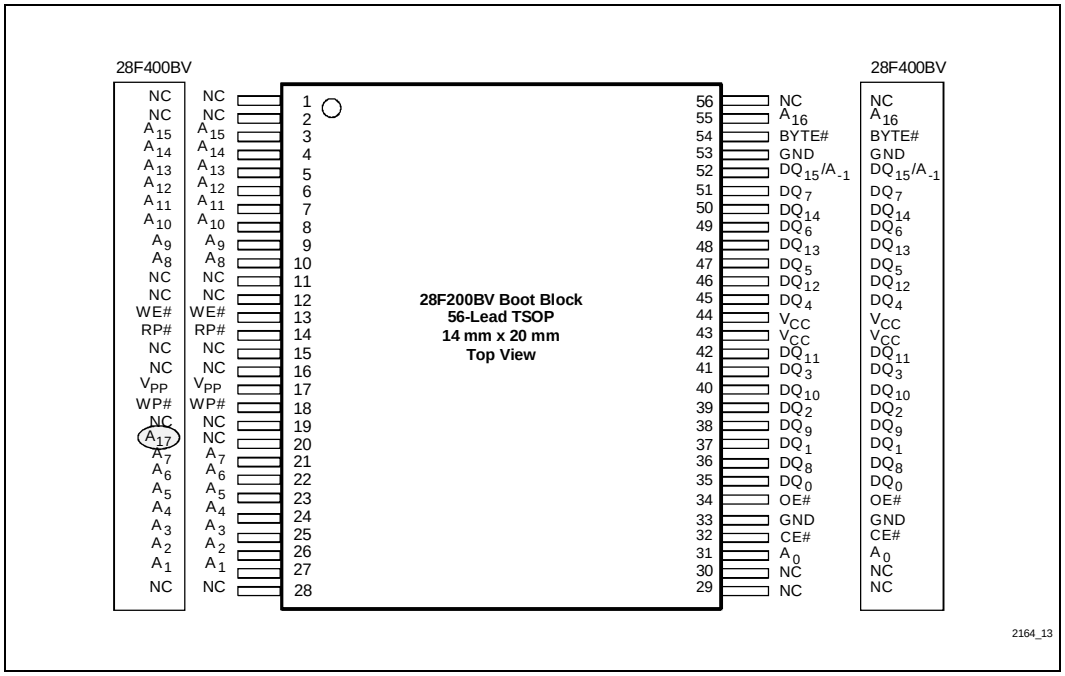


Figure 13. The 56-Lead TSOP Offers Compatibility between 2 and 4 Mbits