AP-607

APPLICATION NOTE

Multi-Site Layout Planning with Intel's FlashFile™ Components, Including ROM Compatibility

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December 1995

ADVANCE INFORMATION

Order Number: 292159-002

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MULTI-SITE LAYOUT PLANNING WITH INTEL'S FlashFile™ COMPONENTS, INCLUDING ROM COMPATIBILITY

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CONTENTS

1.0 INTRODUCTION

With the availability of the 28F016SA/SV and the DD28F032SA, Intel offers a complete FlashFile™ memory family of components. Available in 8-, 16- and 32-Mbit capacities, these components offer flash solutions for applications ranging from mobile computing and communications to embedded code/data storage flash memory systems.

This application note covers the area of designing compatible and/or compact PCB layouts for FlashFile components (see Figure 1 for example). In addition to flexible layouts, flash-to-ROM compatible solutions are provided.

2.0 PINOUT OPTIONS

Whereas the 28F008SA is 8-bit wide, the 28F016SA/SV and DD28F032SA are high-performance, 16-bit wide FlashFile components, offering a user-configurable bus width. Hence, an additional eight I/O pins are on the 28F016SA/SV and DD28F032SA. Furthermore, the implementation of additional features such as write protect, block locking and user-selectable 3.3V and 5.0V operation require control pins for these functions. Additionally, the DD28F032SA has three chip enable pins, compared to two on the 28F016SA/SV, and one on the 28F008SA. In summary, the optimization of the 28F016SA/SV and the DD28F032SA architecture, which achieves high write performance, results in a different pinout configuration from the 28F008SA.

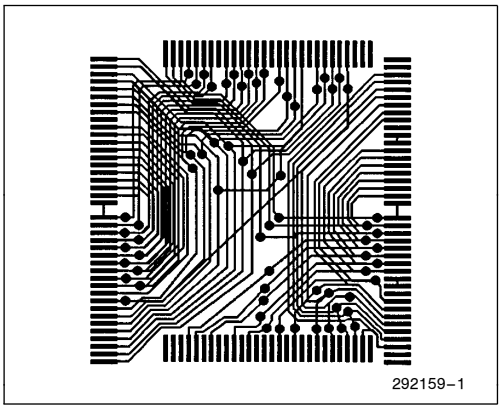

Figure 1. Two Layer Solution for Upgrading from Two 28F008SA to One 28F016SA/SV, FlashFile Component (x8 Mode)

2.1 28F016SA to 28F016SV Pinout Compatibility

The SmartVoltage 16-Mbit 28F016SV is fully pinout-compatible with the 28F016SA. Both SmartVoltage 16-Mbit FlashFile Memory devices use a 56-Lead TSOP and SSOP packages.

3.0 AVAILABLE PACKAGES

The 28F008SA is offered in two packages—the 40-Lead Thin Small Outline Packaging (TSOP), both Standard and Reverse pinout (Figure 2), and the 44-Lead Plastic Small Outline Package (PSOP) (Figure 3). The use of Standard and Reverse TSOP packages arranged in a serpentine layout results in an optimum array density for the 28F008SA (see Section 4.8). The 28F016SA/SV and DD28F032SA are available in Standard 56-Lead TSOP package (see Figure 4). As shown in the examples, the same high density compared to a serpentine layout is achievable with the use of Standard 56-Lead TSOPs arranged in an upright position. The 28F016SA/SV are also available in 56-Lead Shrink Small Outline Package (SSOP) packaging (refer to Figure 5). The 16-Mbit ROM chip used, comes in Standard 44-Lead PSOP and 44-Lead TSOP packages, as shown in Figures 6 and 7, respectively.

4.0 PCB LAYOUTS

Very high-density layouts have been made possible by using Intel's advanced PCMCIA layout specifications. All layouts considered use from two to three layers. Since power and ground are generally connected to their respective planes, V_{CC} and GND pins have been left unconnected.

Solutions are designed using the "PADS" software by Viewlogic Systems, Inc. Of course, the Gerber files generated are industry-standard and can be used on any major PCB layout tool.

Table 1 provides a list of layouts derived along with diagrams and relevant information. For the schematics of these cases, see Section 6.0.

4.1 Compatible Layout for Upgrading from Two 8-Mbit to One 16-Mbit FlashFile Component

This layout deals with two 28F008SAs upgraded to one 28F016SA/SV in 8-bit and 16-bit modes. Two layers are used, with both the 28F008SAs and the 28F016SA/SV residing on layer 1. Figures 8–10 show x16 mode layout diagrams (for x8 mode, see Section 6.0)

Pins CE_0#, BYTE#, 3/5# and WP# have been left unconnected. CE_0# and BYTE# should be connected to the ground plane. In x8 mode, BYTE# pin is grounded, while in x16 mode, it is connected to V_{CC}. Connection of 3/5# and WP# is dependent on system configuration. Consult Intel's 28F016SA/SV data-sheets for complete description of these pins (order numbers 290489 and 290528, respectively).

In x8 mode layout, A_{20} connects to CE# of the upper 8 Mbit. This is a savings of an extra address line.

The enabling of the 28F016SA/SV can either be done directly from the system bus through a decoder or by ANDing the 8-Mbit CE#s and connecting output to CE_1# (for schematics see file 2t8xt1oh.sch (x16 mode) and 2t8t16oh.sch (x8 mode) in Section 6.0). Of course, the final implementation is dependent on the system designer's preference.

Important dimensions are given below (for both x8 and x16 modes):

Feature	Dimension
Total Layout Area	0.709″ sq. (457.28 mm^2)
X, Y	0.836″ , 0.848″ (21.23 mm, 21.54 mm)
Trace Width	0.005″ (0.127 mm)
Via Size	0.025″ (0.635 mm)
Trace to Trace Spacing	0.005″ (0.127 mm)

Table 1. PCB Layout Diagrams and Reference Information

Case	Section
Compatible Layout for Upgrading from Two 8-Mbit (TSOP) to One 16-Mbit (TSOP) FlashFile Component (Both x8 and x16 Cases Considered)	4.1
Compatible Layout for Intel's 16-Mbit (TSOP) FlashFile Component to 16-Mbit ROM Chip (PSOP, TSOP)	4.2
Compact Layout for Intel's 16-Mbit FlashFile Component Using Standard 56-Lead TSOP Pinout	4.3
Compatible Layout for Upgrading from Four 8-Mbit (TSOP) to Two 16-Mbit (TSOP) FlashFile Components (Both x8 and x16 Cases Considered)	4.4
Compatible Layout for Upgrading from Four 8-Mbit (TSOP) to One 32-Mbit (TSOP) FlashFile Component (Both x8 and x16 Cases Considered)	4.5
Compatible Layout for Upgrading from Two 8-Mbit (PSOP) to One 16-Mbit (SSOP) (Both x8 and x16 Cases Considered)	4.6
Compatible Layout for Upgrading from Two 8-Mbit (TSOP) to One 16-Mbit (SSOP) (Both x8 and x16 Cases Considered)	4.7
Serpentine Layout for 8-Mbit FlashFile Component using Standard and Reverse 40-Lead TSOP Pinout	4.8
Compatible Layout for Upgrading from Eight 8-Mbit (TSOP) to Two 32-Mbit (TSOP) FlashFile Components	4.9
Compatible Layout for Upgrading from 16-Mbit (TSOP) to 16-Mbit (SSOP)	4.10

4.2 Compatible Layout for Intel's 16-Mbit FlashFile Component to 16-Mbit ROM Chip

Three cases of layout are considered:

1. 28F016SA (56-Lead TSOP Package) to 16-Mbit ROM (44-Lead TSOP Package) on the same side of the board (see Figures 11–13).
2. Layout with components (56-Lead TSOP 28F016SA to 44-Lead PSOP 16-Mbit ROM) on same side of the board (see Figures 14–16).
3. Chips (56-Lead TSOP 28F016SA to 44-Lead PSOP 16-Mbit ROM) on opposite sides of the board (see Section 6.0 for layout files).

All three cases use two layers.

Pins CE_0#, WE#, 3/5#, RP#, WP# are left unconnected. With the exception of CE_0# (which needs to be grounded), connection of pins depends on the system design parameters.

Since pin D_{15}/A_{-1} acts as the 16th line of data bus during x16 operations, and the lowest address bit during x8 operations, it is connected to both A_0 and D_{15} pins on the 16-Mbit component.

Pins 29 and 30 (both NC) of 28F016SA overlap with the pin 37 (A_{13}) of 16-Mbit ROM in the same side of board layout (see Figures 14–16). From a manufacturing point of view, solder paste stencil has to be optimized for appropriate volume of solder. This ensures proper spacing between adjacent pins.

Important dimensions are given below:

28F016SA (56-Lead TSOP) to 16-Mbit ROM (44-Lead TSOP) same side:

Feature	Dimension
Total Layout Area	0.63″ sq. (405.8 mm^2)
X, Y	0.84″, 0.75″ (21.3 mm, 19.05 mm)
Trace Width	0.005″ (0.127 mm)
Via Size	0.025″ (0.635 mm)
Trace to Trace Spacing	0.005″ (0.127 mm)

28F016SA (56-Lead TSOP) to 16-Mbit ROM (44-Lead PSOP) same side:

For same side of the board:

Feature	Dimension
Total Layout Area	0.587″ sq. (379.3 mm^2)
X, Y	0.524″, 1.12″ (13.31 mm, 28.5 mm)
Trace Width	0.005″ (0.127 mm)
Via Size	0.025″ (0.635 mm)
Trace to Trace Spacing	0.005″ (0.127 mm)

28F016SA (56-Lead TSOP) to 16-Mbit ROM (44-Lead PSOP) opposite side:

Feature	Dimension
Total Layout Area	0.582″ sq. (375.34 mm^2)
X, Y	0.524″, 1.11″ (13.31 mm, 28.20 mm)
Trace Width	0.006″ (0.1524 mm)
Via Size	0.04″ (1.016 mm)
Trace to Trace Spacing	0.006″ (0.1524 mm)

4.3 Compact Layout for Intel's 16-Mbit FlashFile Component Using Standard 56-Lead TSOP Pinout

Highly-dense flash chip array as compact as the serpentine layout of the 28F008SA is achievable with Standard 56-Lead TSOP package using three layers (see Figures 17–20). Additionally, power and ground can be routed on layer 1.

Important dimensions are given below:

Feature	Dimension
Total Layout Area	2.015″ sq. (1300 mm^2)
X, Y	1.736″, 1.161″ (44.1 mm, 29.49 mm)
Trace Width	0.003″ 0.0762 mm)
Via Size	0.025″ (0.635)
Trace to Trace Spacing	0.003″ (0.0762 mm)
Minimum Annular Ring	0.01″ (0.254 mm)

4.4 Compatible Layout for Upgrading from Four 8-Mbit to Two 16-Mbit FlashFile Components

This section describes the layout solution for four 28F008SA to two 28F016SA/SV FlashFile components in x8 and x16 modes. Two layers are used to achieve the desired compactness. Solution is obtained using layout discussed in Section 4.1 twice (see Section 6.0 for layout files).

Important dimensions are given below (for both x8 and x16 modes):

Feature	Dimension
Total Layout Area	1.547″ sq. (998 mm^2)
X, Y	1.75″, 0.884″ (44.45 mm, 22.45 mm)
Trace Width	0.005″ (0.127 mm)
Via Size	0.025″ (0.635 mm)
Trace to Trace Spacing	0.005″ (0.127 mm)

4.5 Compatible Layout for Upgrading from Four 8-Mbit to One 32-Mbit FlashFile Component

Compact layout for upgrading from four 28F008SA to one DD28F032SA FlashFile component in x8 and x16 modes is considered in this section (see Section 6.0 for layout files). Two layers are used.

Important dimensions are given below (for both x8 and x16 modes):

Feature	Dimension
Total Layout Area	1.48″ sq. (956 mm^2)
X, Y	1.75″, 0.847″ (44.45 mm, 21.5 mm)
Trace Width	0.005″ (0.127 mm)
Via Size	0.025″ (0.635 mm)
Trace to Trace Spacing	0.005″ (0.127 mm)

4.6 Compatible Layout for Upgrading from Two 8-Mbit (PSOP Packaging) to One 16-Mbit (SSOP Packaging)

This layout deals with two 28F008SA (in PSOP packaging) upgraded to one 28F016SA/SV (in SSOP packaging) in 8-bit and 16-bit modes. Two layers are used, with the 28F008SAs on layer 1 and the 28F016SA/SV residing on layer 2 (see Section 6.0 for layout files).

For unconnected pin information and details concerning enabling of the chips, consult Section 4.1 (also see schematic file 2t8t16h.sch listed in Section 6.0).

Important dimensions are given below (for both x8 and x16 modes):

Feature	Dimension
Total Layout Area	1.5″ sq. (969 mm^2)
X, Y	1.341″, 1.12″ (34.06 mm, 28.45 mm)
Trace Width	0.005″ (0.127 mm)
Via Size	0.025″ (0.635 mm)
Trace to Trace Spacing	0.005″ (0.127 mm)

4.7 Compatible Layout for Upgrading from Two 8-Mbit (TSOP Packaging) to One 16-Mbit (SSOP Packaging)

This layout deals with two 28F008SA (TSOP packaging) to one 28F016SA/SV (SSOP package) in 8-bit and 16-bit modes. Two layers are used, with the 28F008SAs and the 28F016SA on opposite sides of the board (see Section 6.0 for layout files).

For unconnected pin information and details concerning enabling of the chip, consult Section 4.1.

Important dimensions are given below (for both x8 and x16 modes):

Feature	Dimension
Total Layout Area	0.786″ sq. (507 mm^2)
X, Y	0.836″ , 0.94″ (21.23 mm, 23.9 mm)
Trace Width	0.005″ (0.127 mm)
Via Size	0.025″ (0.635 mm)
Trace to Trace Spacing	0.005″ (0.127 mm)

4.8 Serpentine Layout for 8-Mbit FlashFile Component Using Standard and Reverse 40-Lead TSOP Pinout

This section describes an 8-Mbyte flash memory array using TSOP packaged 28F008SAs in Standard and Reverse configurations (see section 6.0 for layout files). A layout like this is used in Intel's Series 2 flash memory cards and provides optimum array density for available board space. Additionally, two layers are used.

Component RY/BY#s and CE#s are left unconnected.

Important dimensions are given below:

Feature	Dimension
Total Layout Area	3.06″ sq. (1974 mm^2)
X, Y	1.7″ , 1.8″ (43.18 mm, 45.72 mm)
Trace Width	0.005″ (0.127 mm)
Via Size	0.025″ (0.635 mm)
Trace to Trace Spacing	0.005″ (0.127 mm)

4.9 Compatible Layout for Upgrading from Eight 8-Mbit to Two 32-Mbit FlashFile Components

The serpentine layout described in Section 4.8, is used in this solution with slight modifications. Besides performance increase, saving of more than twice the PCB area are achievable when upgrading from 28F008SA to DD28F032SA (see Section 6.0 for layout files). The layout uses two layers.

Important dimensions are given below:

Feature	Dimension
Total Layout Area	3.47″ sq. (2240 mm^2)
X, Y	1.93″ , 1.8″ (49 mm, 45.72 mm)
Trace Width	0.005″ (0.127 mm)
Via Size	0.025″ (0.635 mm)
Trace to Trace Spacing	0.005″ (0.127 mm)

4.10 Compatible Layout for Upgrading from 16-Mbit (TSOP to 16-Mbit (SSOP)

This layout enables easy upgrade from 56-TSOP package to 56-SSOP package. With the exception of NC pins, all pins are connected between the two packages. The layout uses two layers.

Important dimensions are given below:

Feature	Dimension
Total Layout Area	0.953″ sq. (615 mm^2)
X, Y	1.49″ , 0.64″ (37.85 mm, 16.25 mm)
Trace Width	0.005″ (0.127 mm)
Via Size	0.025″ (0.635 mm)
Trace to Trace Spacing	0.005″ (0.127 mm)

5.0 DECOUPLING

To eliminate voltage variations, and thus insuring optimum performance in a high speed environment, use of DECOUPLING capacitors is recommended for FlashFile components. Both main and erase/write power supplies need to be decoupled against DC drifts and switching transients "noise."

For FlashFile components, a 0.1 μF, or greater, multilayer ceramic capacitor per device is recommended. Additional suggestions to obtain good decoupling performance include:

1. The lead length and bond lines (device to capacitor to ground) must be kept to a minimum, since they are a major source of inductance.

2. To increase path numbers (gridding) for reduced inductance and more effective surge-current availability, use one capacitor per chip. This also helps in reducing the lead length and bond lines.

6.0 GENERAL GUIDELINES AND METHODOLOGY FOR DESIGNING COMPATIBLE/COMPACT LAYOUT

Much effort has been made to incorporate most of the common layout combinations. However, for cases not considered here, a set of general guidelines follow to assist in developing solutions. Some of the key points are:

1. Select packages to use.
2. Develop part decals based on dimensions provided by respective vendors. Leave enough pads room to allow for manufacturing tolerances.
3. Select the optimum placement of part decals after trying different combinations.
4. To minimize manufacturing cost, use thick tracks (0.005 inches minimum).
5. Keep via count to a minimum.
6. Use largest vias permitted by the area constraints and process.
7. To reduce signal attenuation and noise, avoid 90° bends in the track routing (instead, use two 45° bends).
8. Use separate planes for ground and power. If limited by number of layers, use thick tracks, two to three times wider than signals track width.

7.0 AVAILABILITY OF FILES

Due to space constraints, the layout diagrams and accompanying schematics for all the cases *are not* included in this application note. However, they are available through Intel's Bulletin Board Service (BBS) under the FlashFile technology area. The number to dial is:

North America and Japan(1)	916-356-3600
Europe	+44(0)1793-496340

NOTE:
1. When calling from Japan, add "01" before the number listed above.

As mentioned before, Gerber files are generated using "PADS" software by Viewlogic Systems, Inc. However, OrCAD® package is used for schematic entry.

Each layout case considered consists of a minimum of four Gerber files (Layer 1, Layer 2, Soldermask 1 and Silkscreen 1) and one schematic file. Additional layers or schematic files might be present in some cases (see Table 2 for filename conventions used).

Table 2. Filename Conventions

Filename	Convention
*Filename*a.*	Layer 1 (Gerber File)
*Filename*b.*	Layer 2 (Gerber File)
*Filename*c.*	Layer 3 (Gerber File)
*Filename*s.*	Silkscreen 1 (Gerber File)
*Filename*t.*	Silkscreen 2 (Gerber File)
*Filename*m.*	Soldermask 1 (Gerber File)
*Filename*n.*	Soldermask 2 (Gerber File)
Filename?h.*	Page 1 (Schematic File)
*Filename*i.*	Page 2 (Schematic File)

The following is a complete list of files present on the BBS:

Index of Layouts/Schematics

File Name	Description	Relevant Section
2t8xt16a.pho	Layout and schematic files for ''two 8-Mbit (TSOP) to one 16-Mbit (TSOP) FlashFile component'' in x16 mode.	4.1
2t8xt16b.pho		4.1
2t8xt16m.pho		4.1
2t8xt16s.pho		4.1
2t8xt16h.sch		4.1
2t8xt1oh.sch		4.1
2t8t16a.pho	Layout and schematic files for ''two 8-Mbit (TSOP) to one 16-Mbit (TSOP) FlashFile component'' in x8 mode.	4.1
2t8t16b.pho		4.1
2t8t16m.pho		4.1
2t8t16s.pho		4.1
2t8t16h.sch		4.1
2t8t16oh.sch		4.1
t16t16sa.pho	Layout and schematic files for ''16-Mbit (TSOP) FlashFile component to 16-Mbit ROM (TSOP)'' on the same side of the board.	4.2
t16t16sb.pho		4.2
t16t16sm.pho		4.2
t16t16ss.pho		4.2
t16t16sh.sch		4.2
t16r16sa.pho	Layout and schematic files for ''16-Mbit (TSOP) FlashFile component to 16-Mbit ROM (PSOP)'' on the same side of the board.	4.2
t16r16sb.pho		4.2
t16r16sm.pho		4.2
t16r16ss.pho		4.2
t16r16sh.sch		4.2
t16r16oa.pho	Layout and schematic files for ''16-Mbit (TSOP) FlashFile component to 16-Mbit ROM (PSOP)'' on the opposite sides of the board.	4.2
t16r16ob.pho		4.2
t16r16om.pho		4.2
t16r16os.pho		4.2
t16r16on.pho		4.2
t16r16ot.pho		4.2
t16r16oh.sch		4.2

NOTE:
Other examples may be added over time.

Index of Layouts/Schematics (Continued)

File Name	Description	Relevant Section
4t16a.pho	Layout and schematic files for ''compact 16-Mbit (TSOP) FlashFile component layout''	4.3
4t16b.pho		4.3
4t16c.pho		4.3
4t16m.pho		4.3
4t16s.pho		4.3
4t16h.sch		4.3
4t8xt16a.pho	Layout and schematic files for ''four 8-Mbit (TSOP) to two 16-Mbit (TSOP) FlashFile components'' in x16 mode.	4.4
4t8xt16b.pho		4.4
4t8xt16m.pho		4.4
4t8xt16s.pho		4.4
4t8xt16h.sch		4.4
4t8xt16i.sch		4.4
4t82t16a.pho	Layout and schematic files for ''four 8-Mbit (TSOP) to two 16-Mbit (TSOP) FlashFile components'' in x8 mode.	4.4
4t82t16b.pho		4.4
4t82t16m.pho		4.4
4t82t16s.pho		4.4
4t82t16h.sch		4.4
4t82t16i.sch		4.4
4t8xt32a.pho	Layout and schematic files for ''four 8-Mbit (TSOP) to one 32-Mbit (TSOP) FlashFile component'' in x16 mode.	4.5
4t8xt32b.pho		4.5
4t8xt32m.pho		4.5
4t8xt32s.pho		4.5
4t8xt32h.sch		4.5
4t8xt32i.sch		4.5
4t8t32a.pho	Layout and schematic files for ''four 8-Mbit (TSOP) to one 32-Mbit (TSOP) FlashFile component'' in x8 mode.	4.5
4t8t32b.pho		4.5
4t8t32m.pho		4.5
4t8t32s.pho		4.5
4t8t32h.sch		4.5
4t8t32i.sch		4.5

NOTE:
Other examples may be added over time.

Index of Layouts/Schematics (Continued)

File Name	Description	Relevant Section
2p8xs16a.pho	Layout and schematic files for ‘‘two 8-Mbit (PSOP) to one 16-Mbit (SSOP) FlashFile component’’ in x16 mode.	4.6
2p8xs16b.pho		4.6
2p8xs16m.pho		4.6
2p8xs16s.pho		4.6
2p8xs16n.pho		4.6
2p8xs16t.pho		4.6
2p8xs16h.sch		4.6
2p8s16a.pho	Layout and schematic files for ‘‘two 8-Mbit (PSOP) to one 16-Mbit (SSOP) FlashFile component’’ in x8 mode.	4.6
2p8s16b.pho		4.6
2p8s16m.pho		4.6
2p8s16s.pho		4.6
2p8s16n.pho		4.6
2p8s16t.pho		4.6
2p8s16h.sch		4.6
2t8xs16a.pho	Layout and schematic files for ‘‘two 8-Mbit (TSOP) to one 16-Mbit (SSOP) FlashFile component’’ in x16 mode.	4.7
2t8xs16b.pho		4.7
2t8xs16m.pho		4.7
2t8xs16s.pho		4.7
2t8xs16n.pho		4.7
2t8xs16t.pho		4.7
2t8xs16h.sch		4.7
2t8s16a.pho	Layout and schematic files for ‘‘two 8-Mbit (TSOP) to one 16-Mbit (SSOP) FlashFile component’’ in x8 mode.	4.7
2t8s16b.pho		4.7
2t8s16m.pho		4.7
2t8s16n.pho		4.7
2t8s16s.pho		4.7
2t8s16t.pho		4.7
2t8s16h.sch		4.7

NOTE:
Other examples may be added over time.

Index of Layouts/Schematics (Continued)

File Name	Description	Relevant Section
8t8a.pho	Layout and schematic files for ''serpentine layout for 8-Mbit (TSOP) FlashFile component.''	4.8
8t8b.pho		4.8
8t8m.pho		4.8
8t8s.pho		4.8
8t8h.sch		4.8
8t82t32a.pho	Layout and schematic files for ''eight 8-Mbit (TSOP) to two 32-Mbit (TSOP) FlashFile components'' in x8 mode.	4.9
8t82t32b.pho		4.9
8t82t32m.pho		4.9
8t82t32s.pho		4.9
8t82t32h.sch		4.9
8t82t32i.sch		4.9
t16s16a.pho	Layout and schematic files for ''one 16-Mbit (TSOP) to one 16-Mbit (SSOP) FlashFile component.''	4.10
t16s16b.pho		4.10
t16s16m.pho		4.10
t16s16s.pho		4.10
t16s16h.sch		4.10

NOTE:
Other examples may be added over time.

8.0 SUMMARY

This application note summarizes highly-dense layout solutions, based on the design constraints such as compatibility and compactness. Different permutations of FlashFile components and 16-Mbit ROM are provided. Furthermore, compact layouts for 16-Mbit array are designed and found to be comparable in PCB layout area to the serpentine layout. This application note, however, *does not* deal with software changes associated with compatibility issues. See AP-375, "Upgrade Considerations from the 28F008SA to the 28F016SA" and AP-393, "28F016SV Compatibility with 28F016SA" for more information on the subject.

9.0 ADDITIONAL INFORMATION

For software upgrade and additional design information, consult the referenced documents listed below:

9.1 References

Order Number	Document
290490	DD28F032SA Datasheet
290489	28F016SA Datasheet
290528	28F016SV Datasheet
290429	28F008SA Datasheet
297372	''16-Mbit Flash Product Family User's Manual''
292092	AP-357, ''Power Supply Solutions for Flash Memory''
292095	AP-360, ''28F008SA Software Drivers''
292097	AP-362, ''Implementing Mobile PC Designs using High-Density FlashFile™ Components''
292123	AP-374, ''Flash Memory Write Protection Techniques''
292124	AP-375, ''Upgrade Considerations from the 28F008SA to the 28F016SA''
292126	AP-377, ''16-Mbit Flash Product Family Software Drivers, 28F016SA/SV/XS/XD''
292127	AP-378, ''System Optimization using Enhanced Features of the 28F016SA''
292144	AP-393, ''28F016SV Compatibility with 28F016SA''
292163	AP-610, ''Flash Memory In-System Code and Data Update Techniques''
292165	AB-62, ''Compiled Code Optimizations for Flash Memories''
294011	ER-27, ''The Intel 28F008SA Flash Memory''
294016	ER-33, ''ETOX™ IV Flash Memory Technology: Insight to Intel's Fourth Generation Process Innovation''
297508	FLASHBuilder Utility
Contact Intel/Distribution Sales Office	Flash Cycling Utility
Contact Intel/Distribution Sales Office	28F016SV iBIS Models
Contact Intel/Distribution Sales Office	28F016SV VHDL Model
Contact Intel/Distribution Sales Office	28F016SV Timing Designer Library Files
Contact Intel/Distribution Sales Office	28F016SV Orcad and ViewLogic Schematic Symbols

9.2 Revision History

Number	Description
-001	Original Version
-002	Added 3/5# pin to Figures 4 and 5; Updated Sections 2.1 and 4.1 accordingly. Updated ''Additional Information'' Section Minor cosmetic changes throughout document.

APPENDIX A
FIGURES

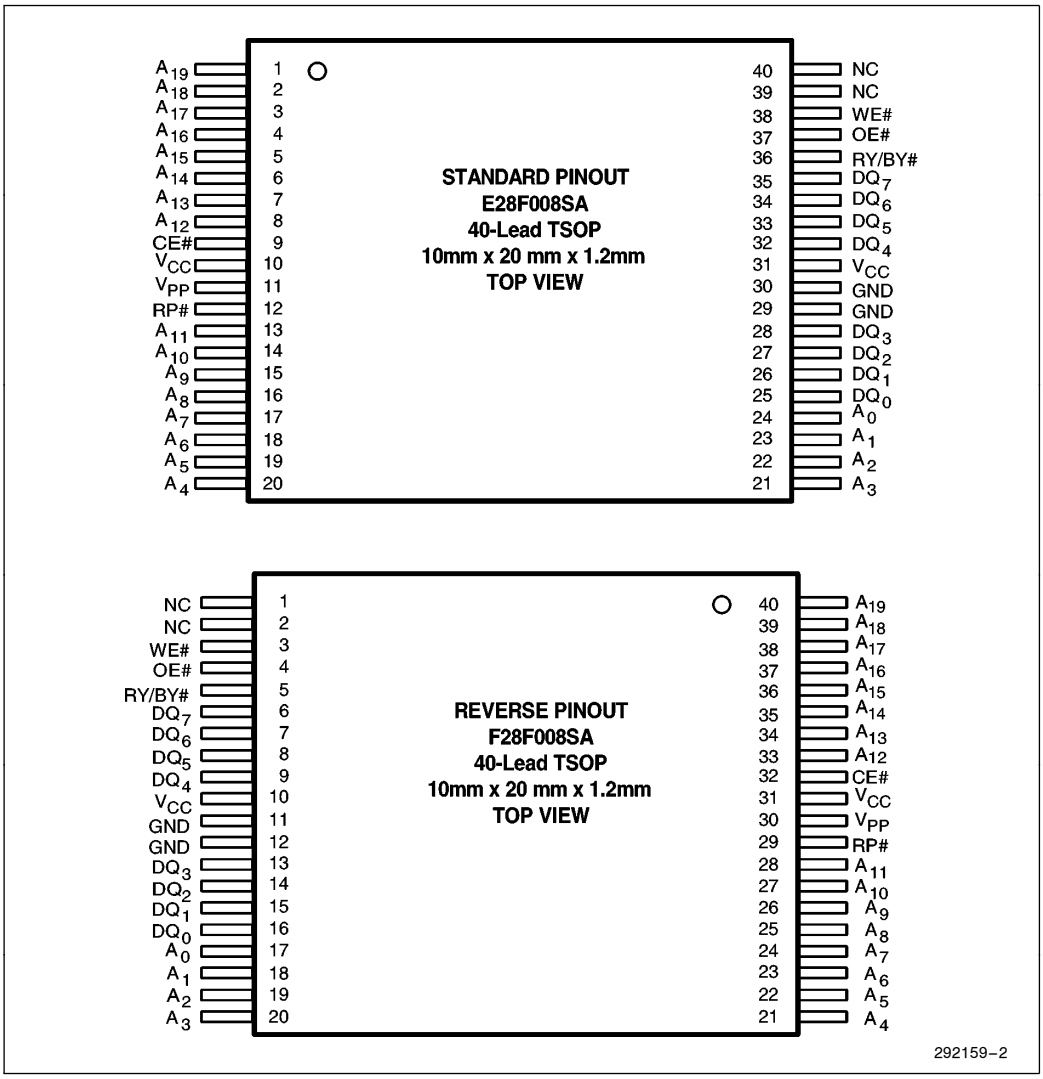

Figure 2. 28F008SA Standard and Reverse 40-Lead TSOP Pinout Configuration

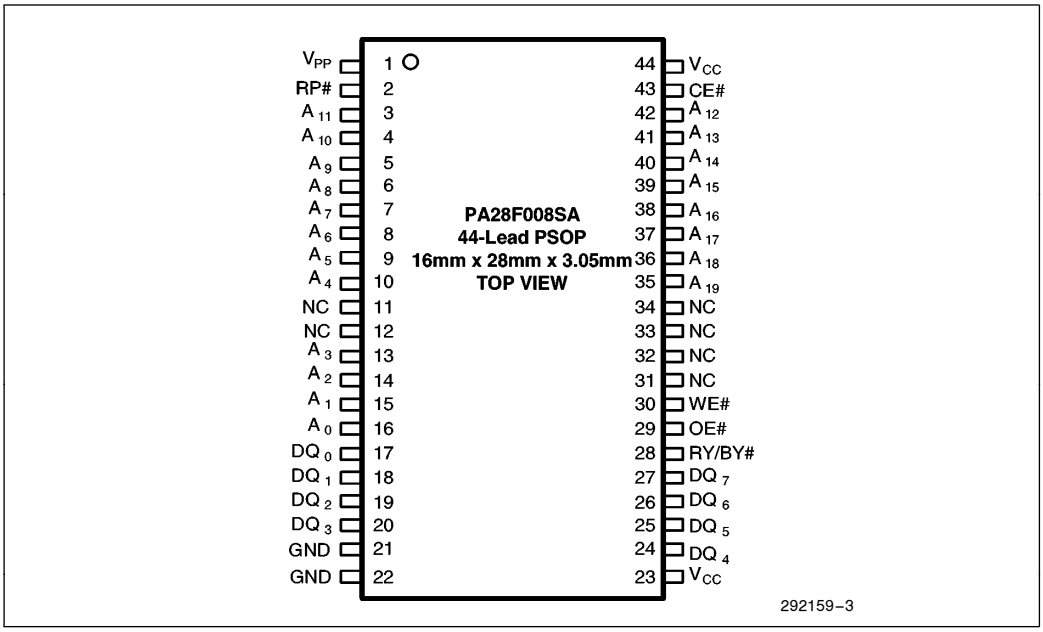

Figure 3. 28F008SA 44-Lead PSOP Pinout Configuration

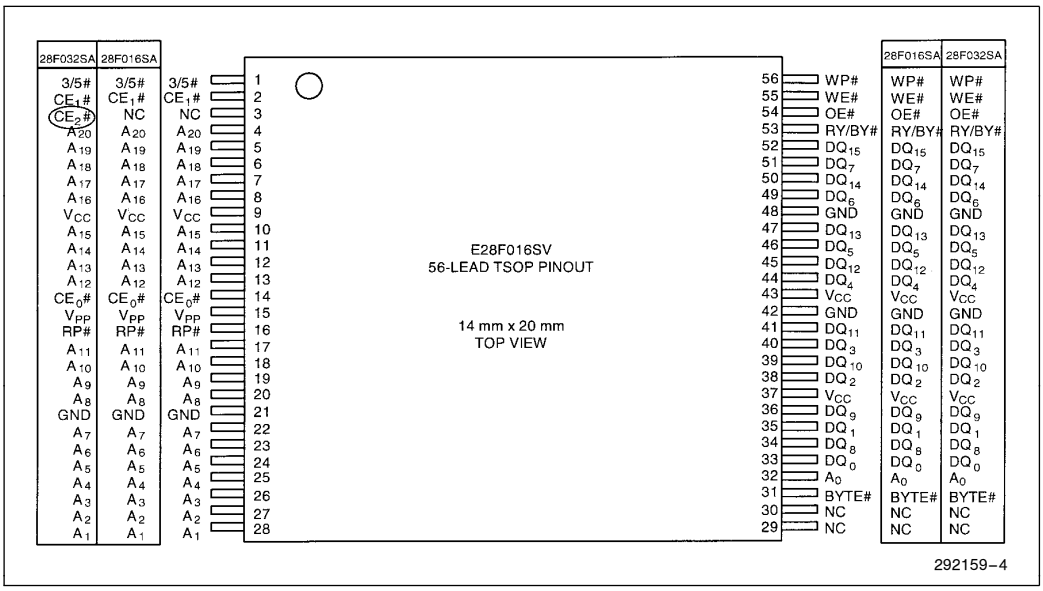

Figure 4. 28F016SA, 28F016SV and DD28F032SA 56-Lead TSOP Pinout Configurations

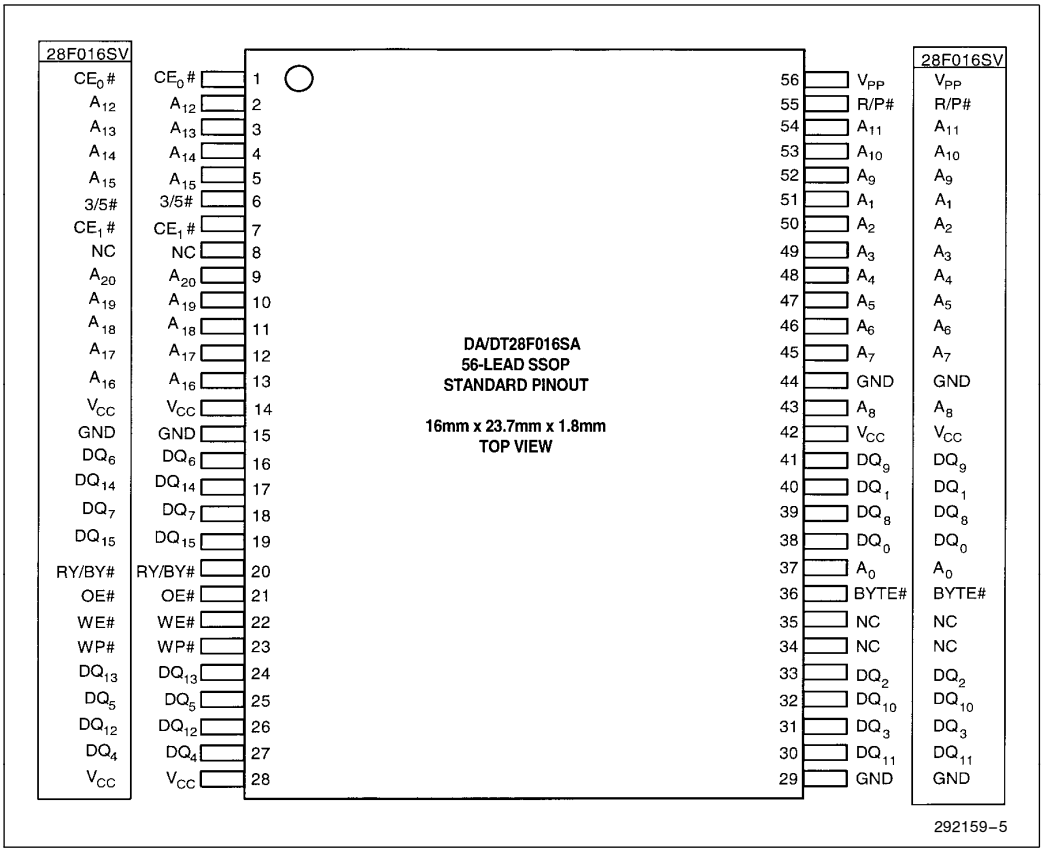

Figure 5. 28F016SA/SV 56-Lead SSOP Pin Configuration

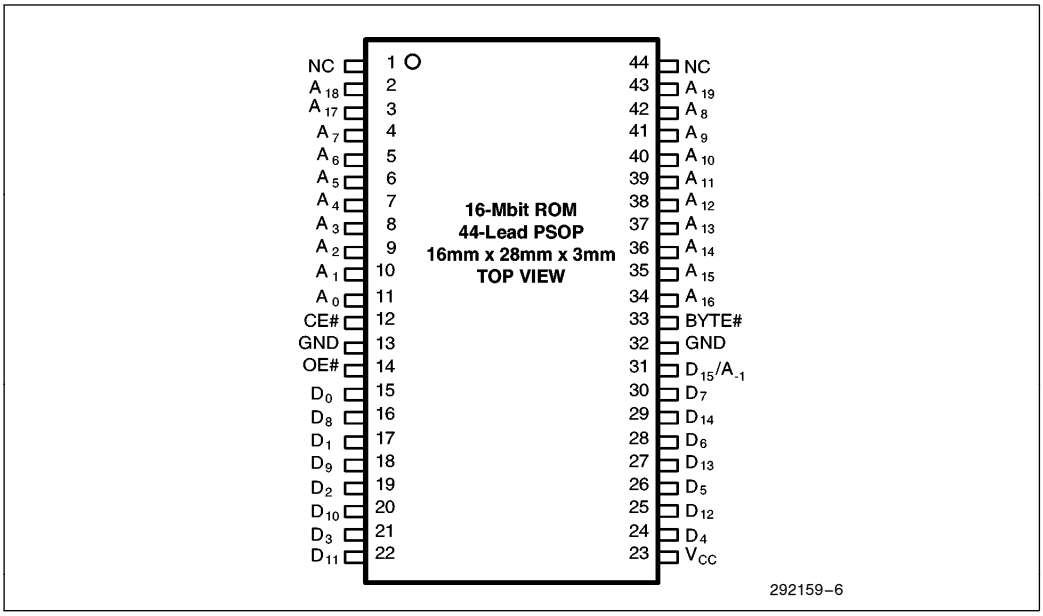

Figure 6. 16-Mbit ROM Chip 44-Lead PSOP Pinout Configuration

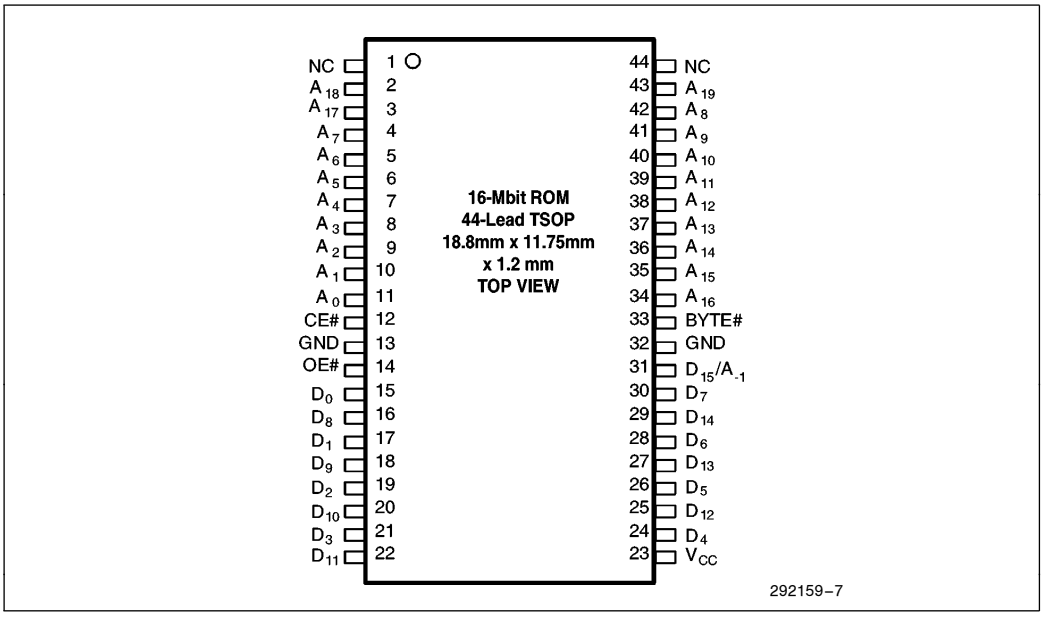

Figure 7. 16-Mbit ROM Chip 44-Lead TSOP Pinout Configuration

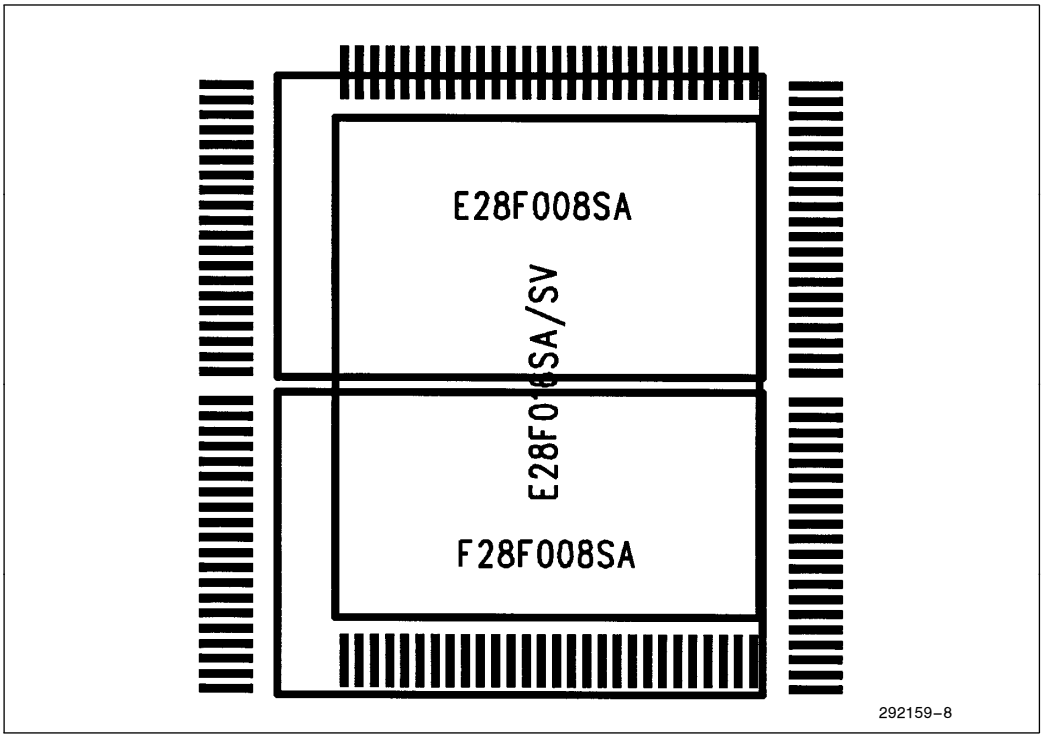

Figure 8. 4x Scale Topside Outline View of *Two 28F008SAs to One 28F016SA/SV (x16 Mode)*

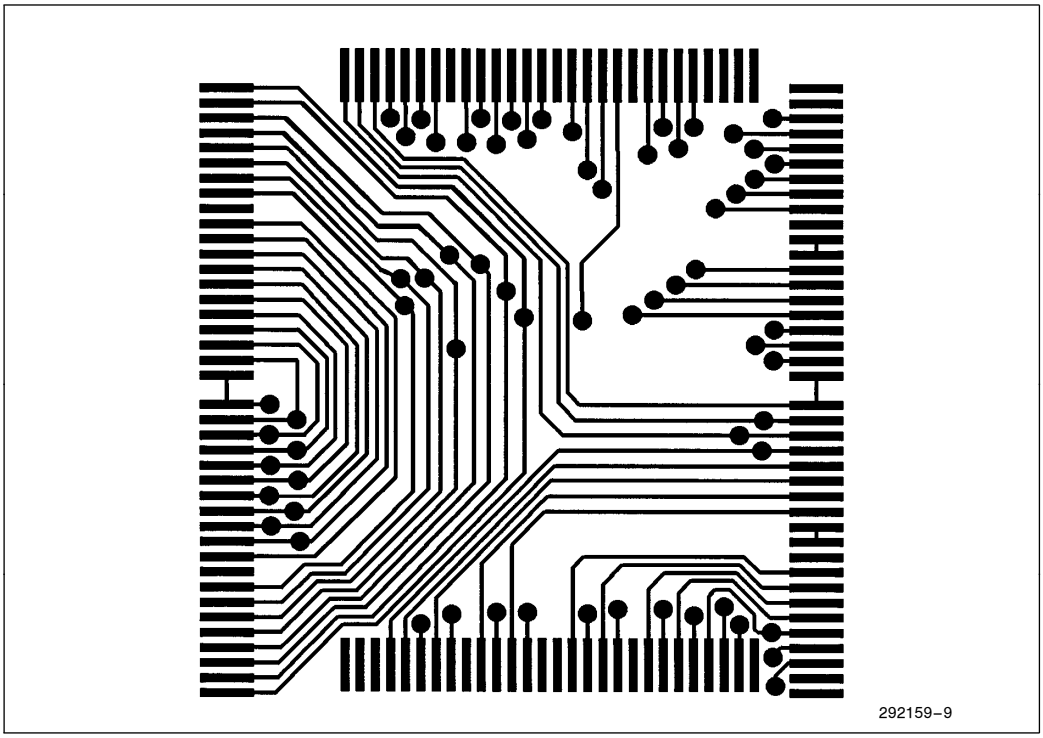

Figure 9. 4x Scale Topside Trace View of *Two 28F008SAs to One 28F016SA/SV (x16 Mode)*

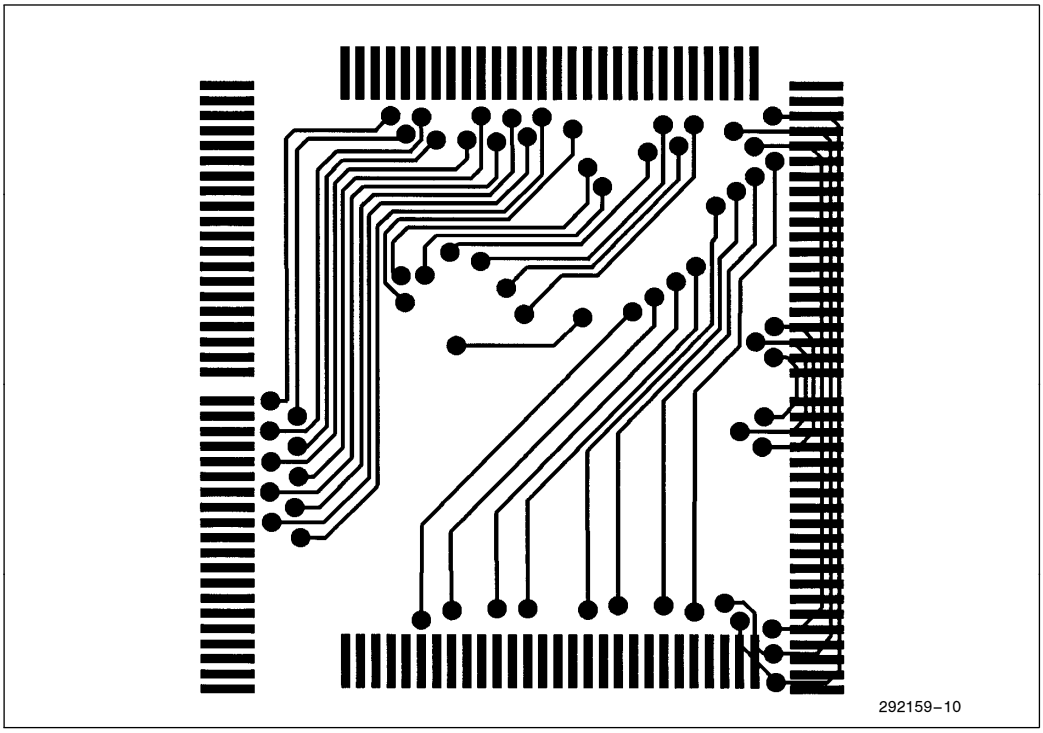

Figure 10. 4x Scale Bottom Side Trace View of *Two 28F008SAs to One 28F016SA/SV (x16 Mode)*

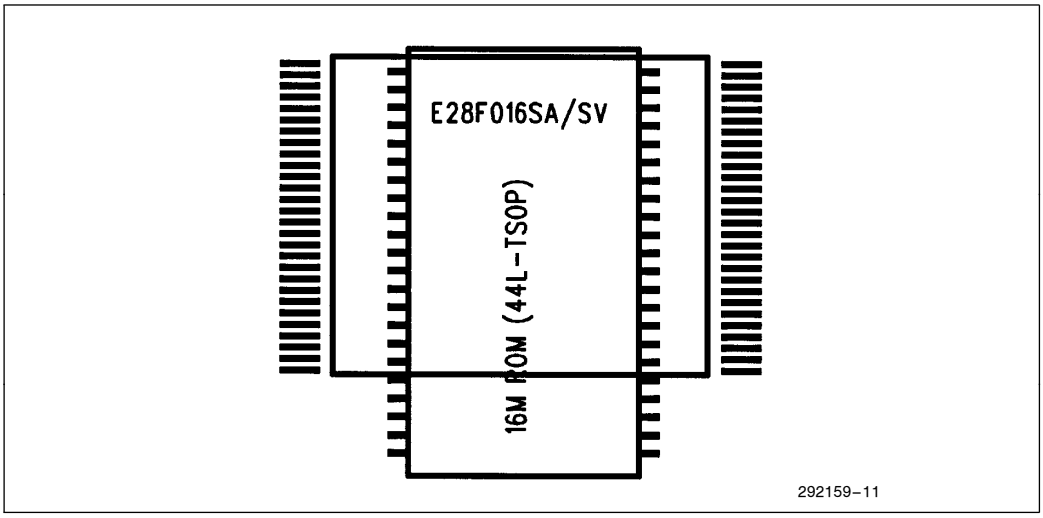

Figure 11. 3x Scale Top Side Outline View of *One 28F016SA/SV (56-Lead TSOP) to One 16-Mbit ROM (44-Lead TSOP)*

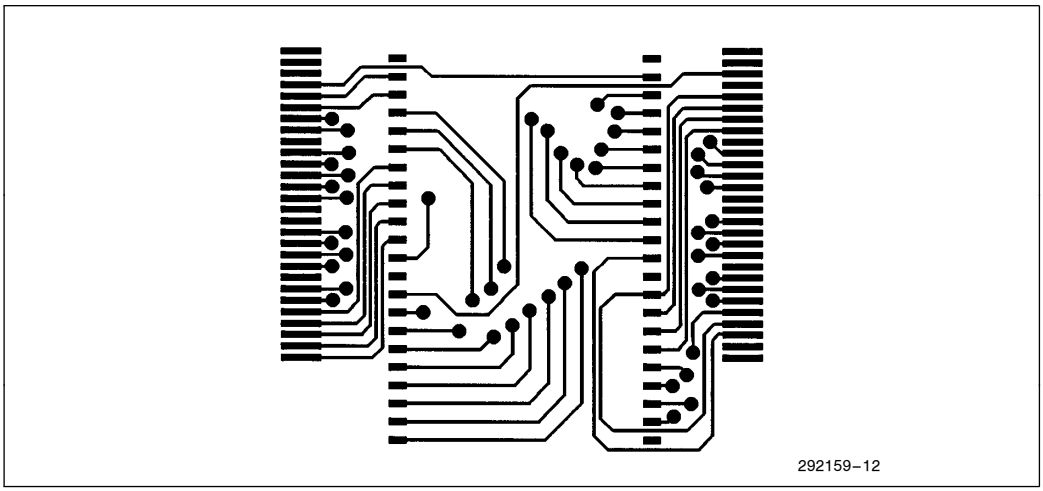

Figure 12. 3x Scale Top Side Trace View of *One 28F016SA/SV (56-Lead TSOP) to One 16-Mbit ROM (44-Lead TSOP)*

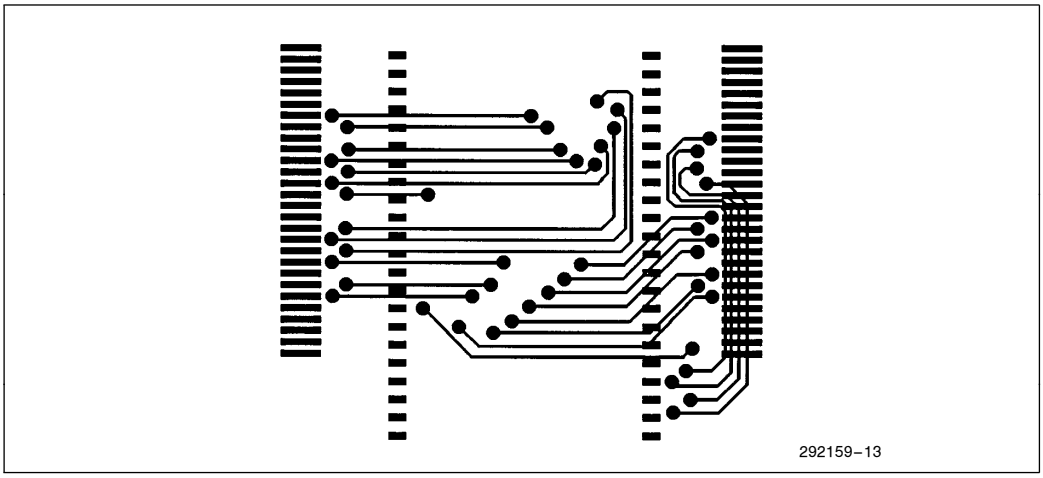

Figure 13. 3x Scale Bottom Side Trace View of *One 28F016SA/SV (56-Lead TSOP) to One 16-Mbit ROM (44-Lead TSOP)*

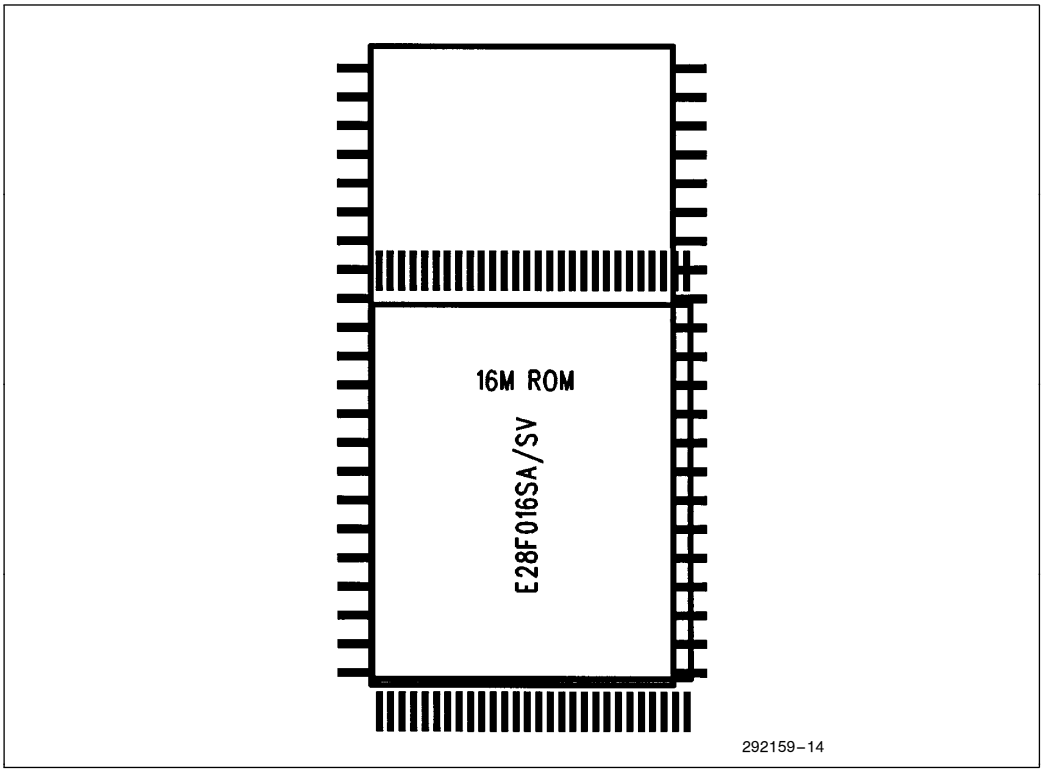

Figure 14. 3x Scale Top Side Outline View of *One 28F016SA/SV (56-Lead TSOP) to One 16-Mbit ROM (44-Lead PSOP)*

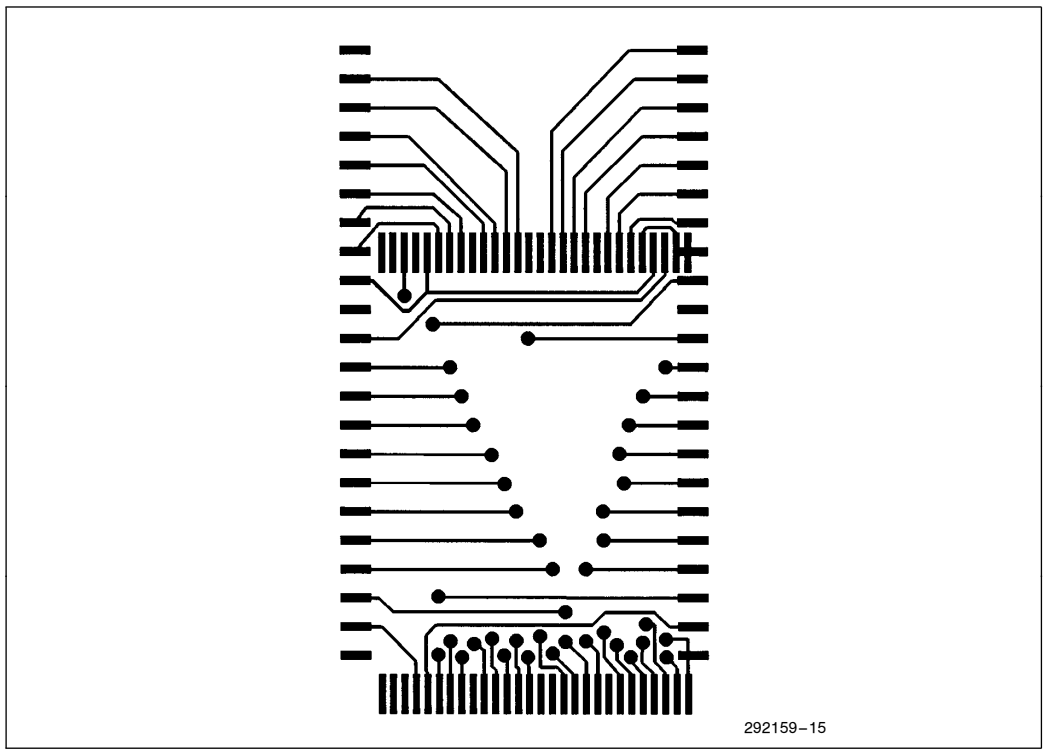

Figure 15. 3x Scale Top Side Trace View of *One 28F016SA/SV (56-Lead TSOP) to One 16-Mbit ROM (44-Lead PSOP)*

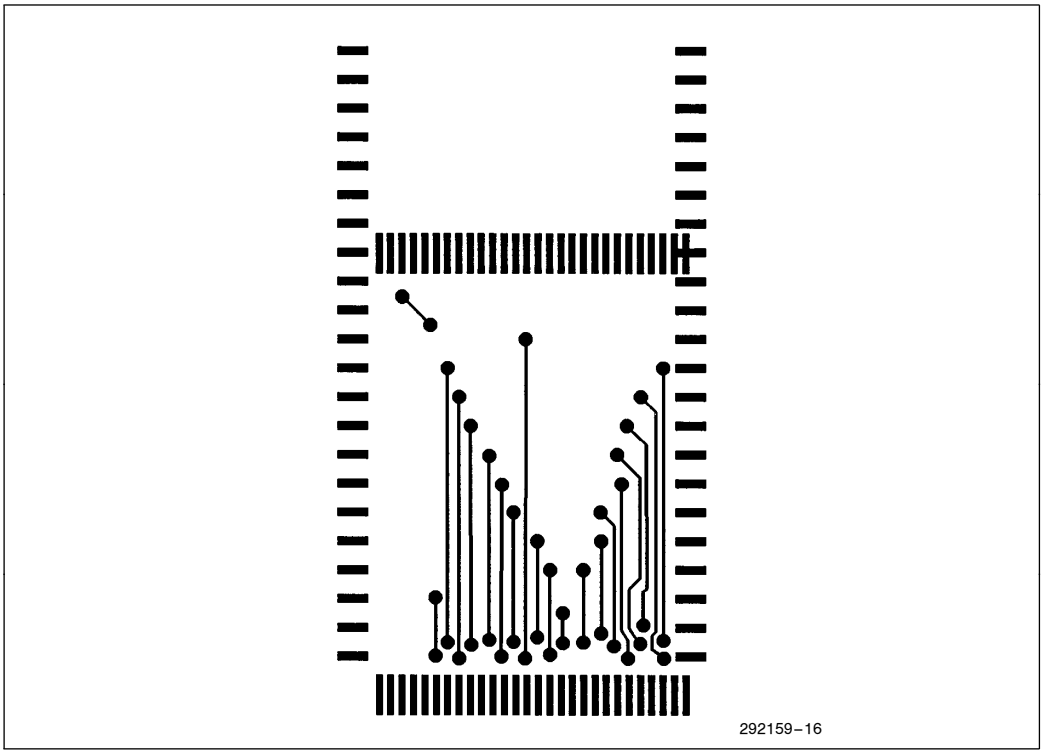

Figure 16. 3x Scale Bottom Side Trace View of *One 28F016SA/SV (56-Lead TSOP) to One 16-Mbit ROM (44-Lead PSOP)*

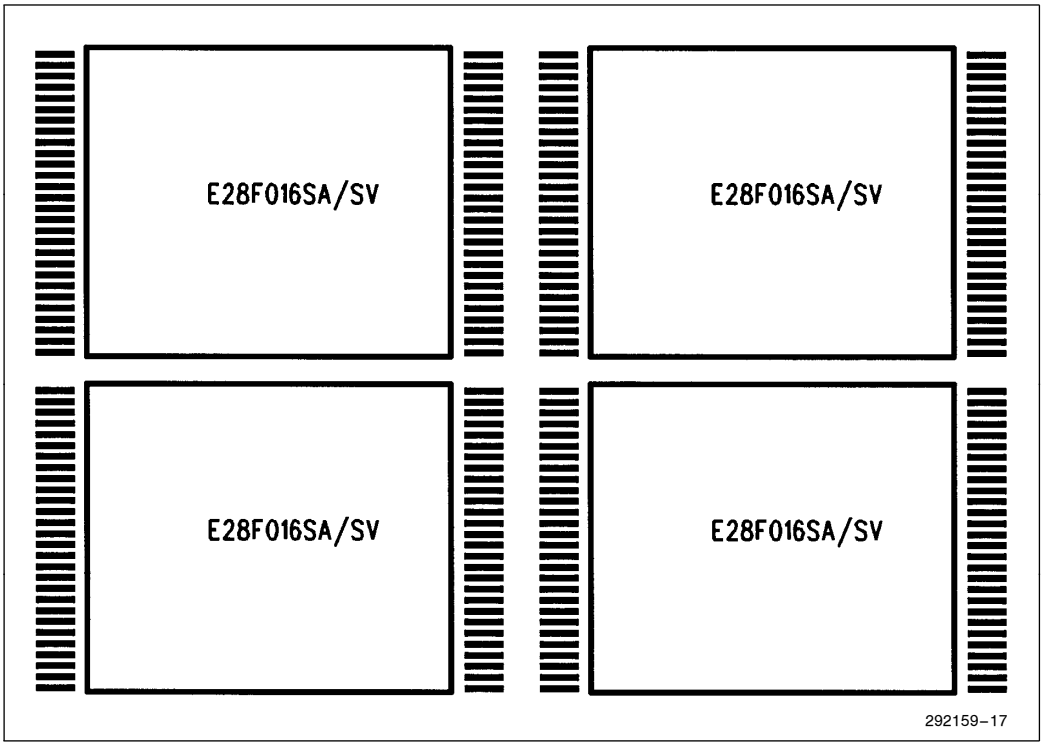

Figure 17. 3x Scale Top Side Outline View of *Four 28F016SA/SVs*

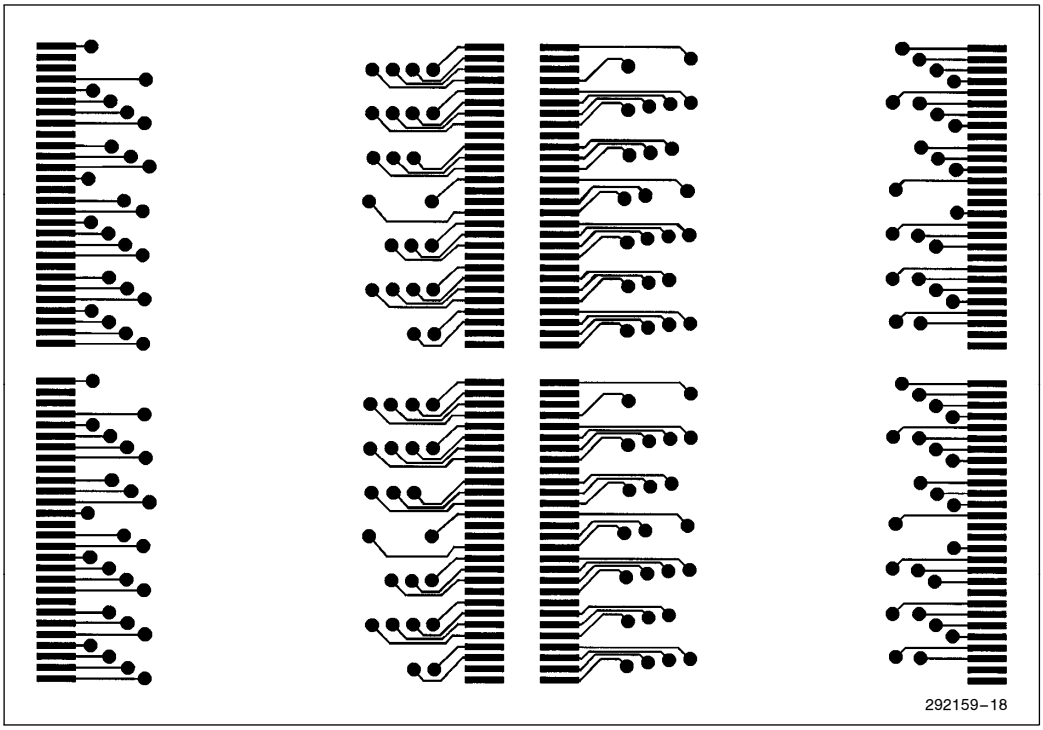

Figure 18. 3x Scale Top Side Trace View of *Four 28F016SA/SVs*

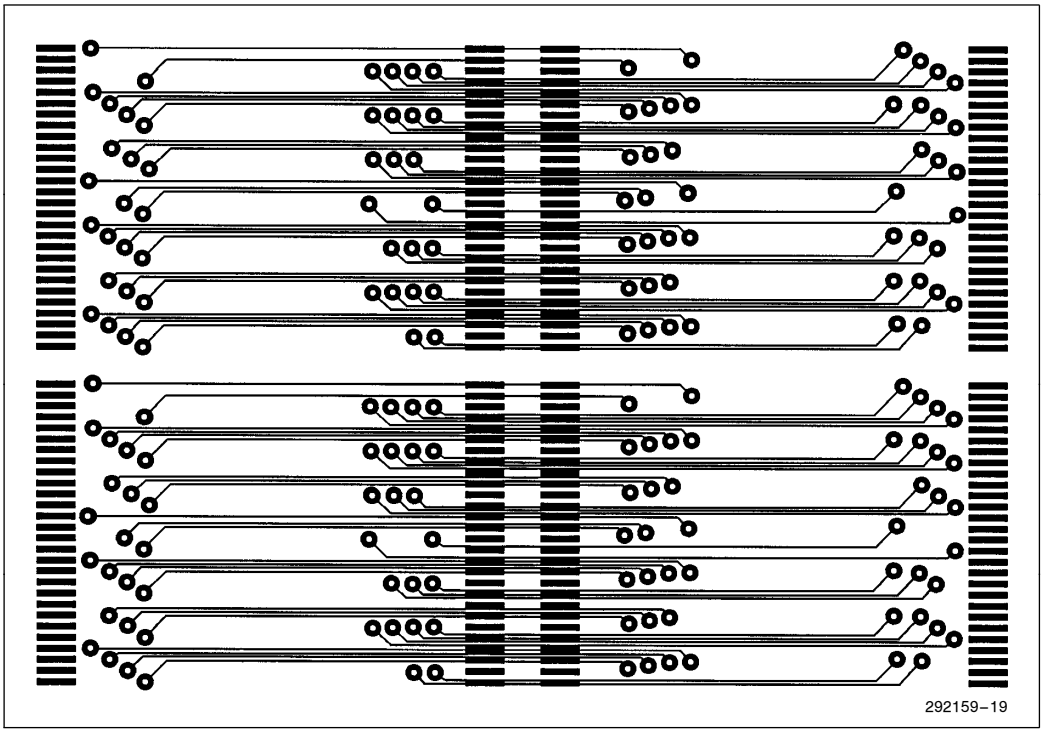

Figure 19. 3x Scale Internal Layer View of *Four 28F016SA/SVs*

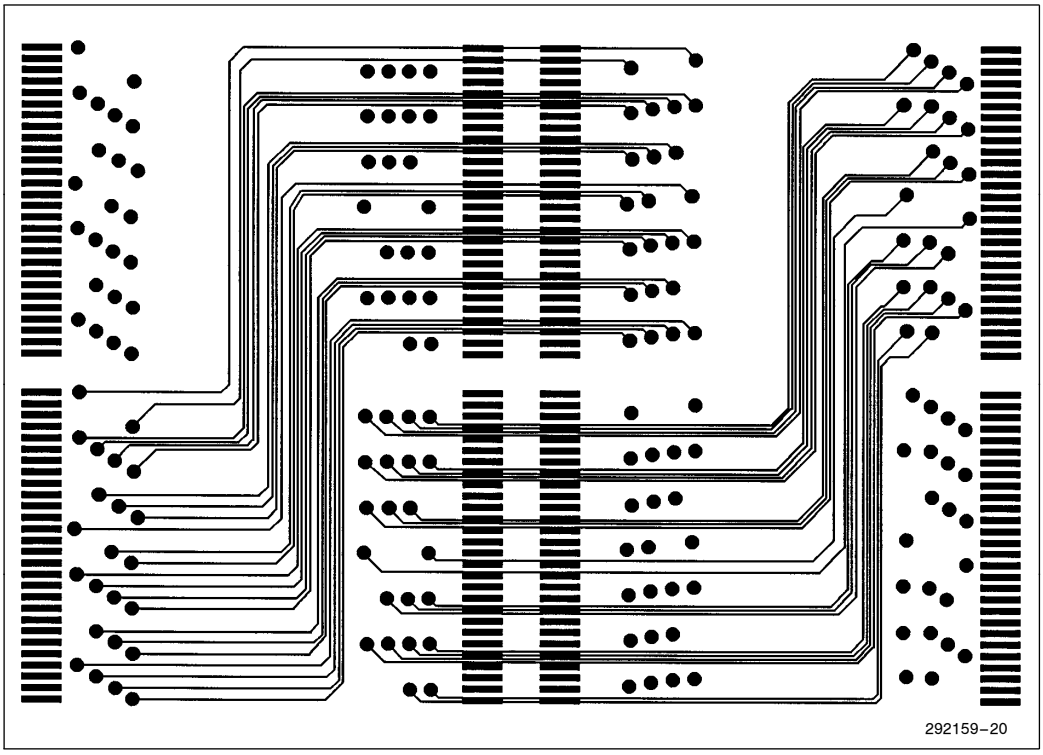

Figure 20. 3x Scale Bottom Side Trace View of *Four 28F016SA/SVs*