AP-600

APPLICATION NOTE

Performance Benefits and Power/Energy Savings of 28F016XS-Based System Designs

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1.0 INTRODUCTION

Microprocessors today have achieved tremendous levels of performance, with year-to-year gains more exponential than linear in nature. Unfortunately, computer systems have not achieved similar performance leaps. Their performance ties not only to the CPU, but is a composite of all computing subsystems; memory, mass storage, video, networking, etc. See Figure 1 for a block diagram of the traditional Von Neumann-based computing architecture.

Memory, the first-line link between the CPU and the mass storage subsystem, feeds the microprocessor with code and data necessary to do useful work. In this capacity, memory directly impacts system performance. Until the CPU receives the code or data it needs, the system stalls.

Figure 2 charts microprocessor performance gains over the last two decades, with Figure 3 showing comparative SRAM and DRAM read performance gains for the same time frame. The difference in the slopes of the three curves is obvious and striking. To optimize the CPU-memory interface and minimize CPU performance impact, system designers are resorting to more and more complex multi-memory architectures (see Figure 4 for an example). This complexity results in added system cost, higher power consumption, lower reliability and ruggedness, larger size and greater weight.

What can be done to solve this apparent paradox? How can a system designer address higher performance while simultaneously simplifying the memory architecture, lowering cost, reducing power consumption, increasing reliability and decreasing form factor/weight? The answer lies not in evolutionary, incremental improvements to existing system architectures, but in revolutionary new architectures based on an equally revolutionary memory alternative, high-density flash memory. Figure 5 shows an example of such a system architecture.

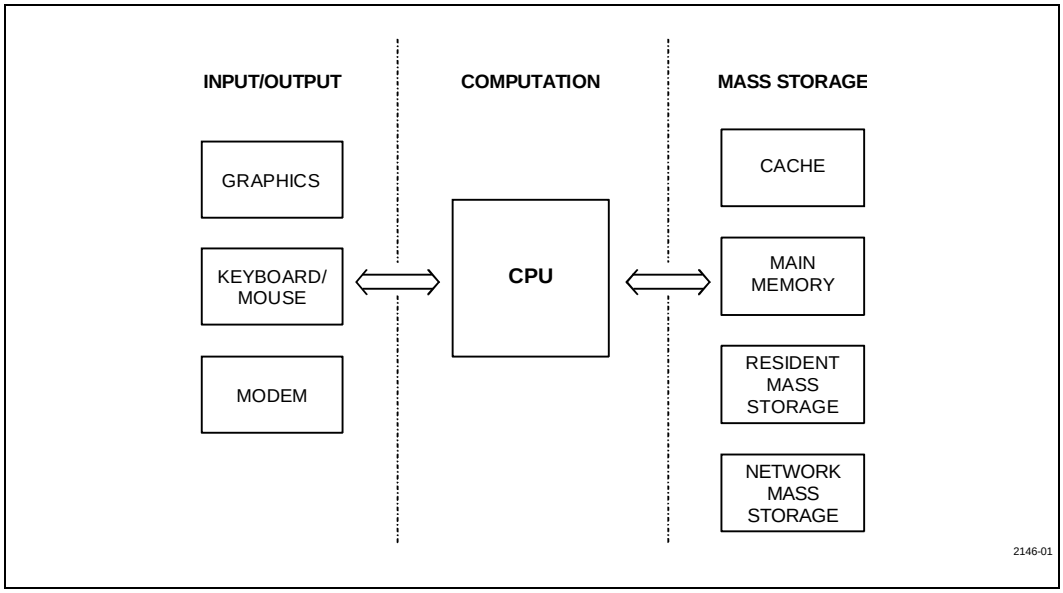

Figure 1. High System Performance Depends on Optimized Operation of All Sub-Systems

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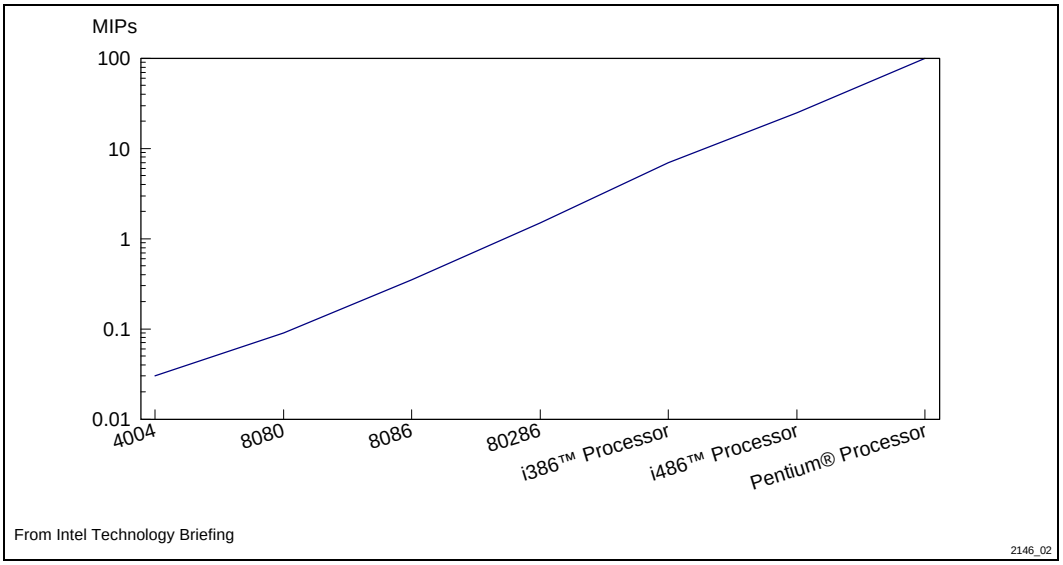

Figure 2. Microprocessor Performance Dramatically Improves with Each New Generation

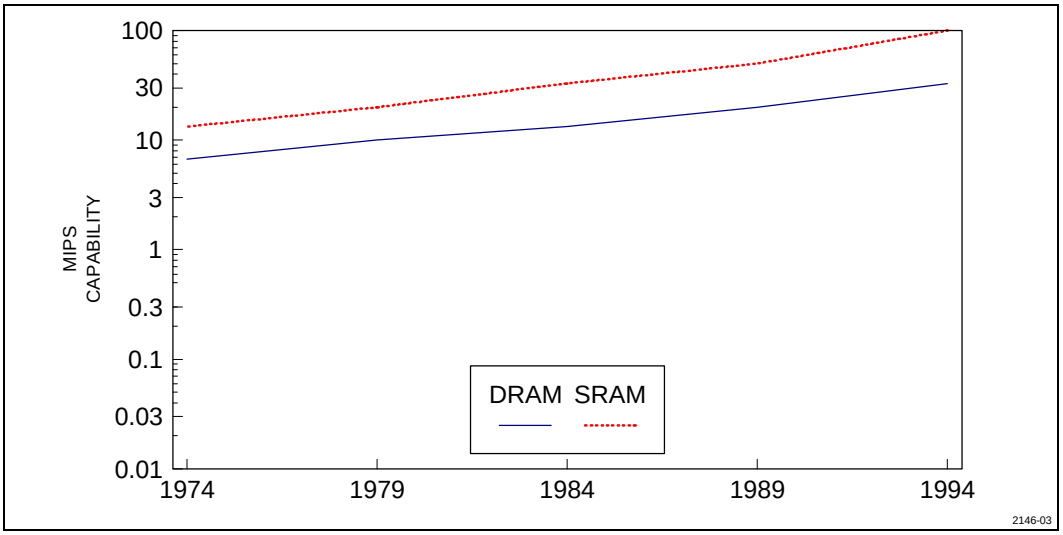

Figure 3. Memory Read Performance Improvements Lag behind Those of Microprocessors

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This application note compares the read performance and power consumption of Intel's 28F016XS flash memory to that of more traditional memory alternatives, based on specifications available at the time this document was published. The 28F016XS flash memory is a new member of the Intel 16-Mbit flash memory product family. Significant 28F016XS enhancements compared to previous flash memories include:

- A synchronous pipelined read interface that optimizes the performance of today's leading-edge microprocessors and buses, and
- SmartVoltage technology

This analysis focuses on the highest read performance versions of the highest-density products for each memory technology. Also discussed are 28F016XS-based system memory architecture advantages over traditional alternatives in terms of performance, complexity, cost, power consumption and reliability. For complete information on Intel's 28F016XS flash memory, consult documentation listed in the Additional Information section.

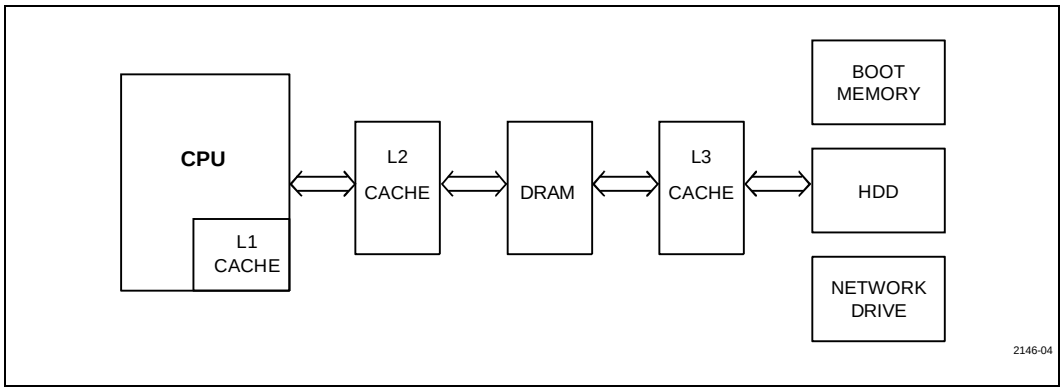

Figure 4. The Traditional System Memory Architecture Adds Complexity in Order to Optimize Performance

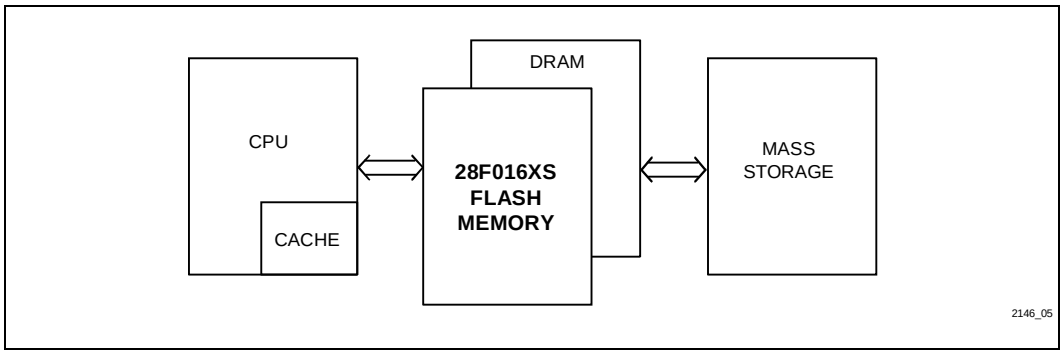

Figure 5. A Flash Memory-Based System Memory Architecture Achieves Performance without Tradeoffs

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2.0 MEMORY PERFORMANCE AND POWER/ENERGY COMPARISONS

This section compares read performance and power/energy consumption in various operating modes for the following memory technologies:

- 28F016XS flash memory (x16)
- 16-Mbit DRAM (x16)
- 4-Mbit SRAM (two x8)
- 1-Mbit cache SRAM (two x8)
- 16-Mbit paged mask ROM (x16)
- 4-Mbit EPROM (x16)
- 1-Mbit EEPROM (x16)
- 1.8" HDD
- 1.3" HDD

In all cases, representative specifications drawn from a composite of multiple memory vendors (when possible) were used.

2.1 Background

The detailed analyses in the Appendix show read performance both in terms of number of clocks and number of wait-states, for a sequence of 256 sequential word (16 bit) reads at 33 MHz. This sequence length was chosen for compatibility with the 512 byte sector size of a HDD. Different sequence lengths will result in different analysis results. Performance calculations measure time from when the memory receives a valid address until it outputs desired data. They do not take into account any additional delays due to bus complexity (address generation, parity checking, etc.) or glue logic (chip select decode, control signal generation, etc.). Read performance calculations also do not include improvements from system design techniques such as multi-bank interleaving.

Calculations show power consumption in three operating modes, read, standby and sleep (if offered), using maximum current specifications and CMOS levels. Read *power* consumption calculations use the highest-specified read frequency. Read *energy* consumption calculations multiply read power consumption by the amount of time required to read the eight word sequence. Therefore, the analysis focuses on read energy consumption, versus read power consumption, to compare relative battery drain for each memory technology during reads.

2.2 The Results

Tables 1-4 and Figures 6-9 summarize the results of these comparisons, with detailed analysis in the Appendix. Section 3 will translate the 28F016XS component strengths into system-level advantages.

Read Performance

As Figure 6 reveals, the 28F016XS read performance approaches that of cache SRAM and exceeds that of all other memory technologies, including DRAM. The 28F016XS is significantly faster than any nonvolatile memory technology. Subsequent tables and figures point out that this performance comes with minimal power penalty compared to alternative memories.

Table 1. Read Performance Comparisons (8-Word Transfers at 33 MHz)

Memory Technology	5.0V V_{CC} Read Transfer Rate (Byte/sec)	5.0V Read Transfer Rate Compared to the 28F016XS	3.3V V_{CC} Read Transfer Rate (Byte/sec)	3.3V Read Transfer Rate Compared to the 28F016XS
28F016XS Flash Memory (x16)	66.1×10^6	1x	44.3×10^6	1x
16-Mbit DRAM (x16)	33.3×10^6	0.50x	33.3×10^6	0.75x
4-Mbit SRAM (two x8)	33.3×10^6	0.50x	16.7×10^6	0.38x
1-Mbit Cache SRAM (two x8)	66.7×10^6	1.01x	66.7×10^6	1.51x
16-Mbit Paged Mask ROM (x16)	19×10^6	0.29x	14×10^6	0.32x
4- Mbit EPROM (x16)	13.3×10^6	0.20x	9.5×10^6	0.21x
1- Mbit EEPROM (x16)	16.7×10^6	0.25x	9.5×10^6	0.21x
1.8" HDD	16.8×10^3	<<	N/A	N/A
1.3" HDD	32.7×10^3	<<	N/A	N/A

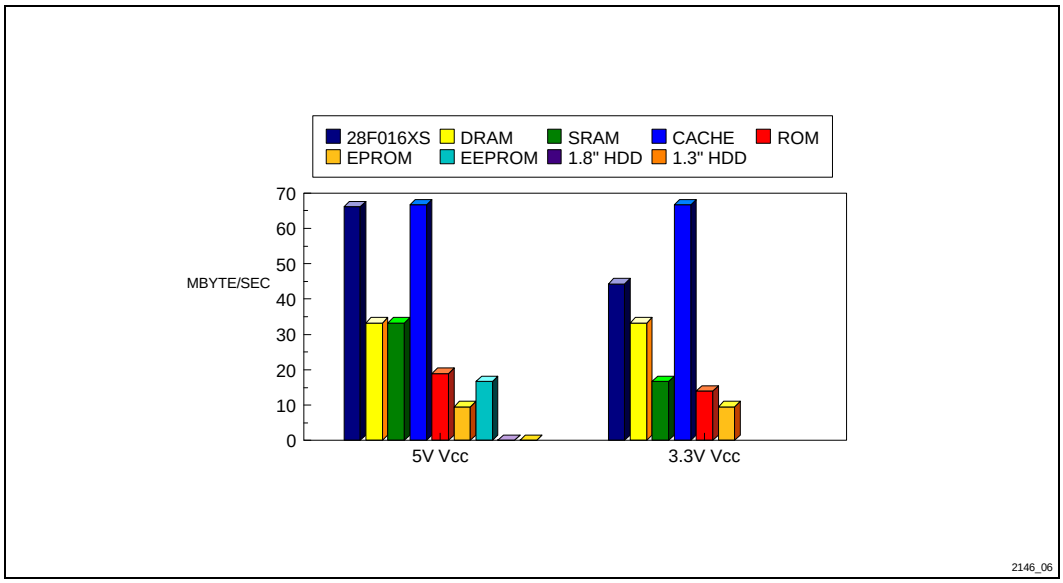

Figure 6. 28F016XS 33 MHz Read Performance Exceeds DRAM, Approaches L2 Cache

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Read Energy Consumption

The 28F016XS's high performance (how long it takes to read a sequence of data words), combined with its low power consumption (how much current is consumed at 5.0V/3.3V V_{CC} to complete the read) give it the lowest read energy consumption of any memory technology. HDD was not included in Figure 7 due to its extraordinarily high power and energy consumption. Unlike the 28F016XS, cache SRAM has a poor power/performance ratio. Its high read transfer rate comes at a significant power price and results in very large read energy consumption.

Table 2. Read Energy Consumption Comparisons (8-Word Transfers at 33 MHz)

Memory Technology	5.0V V_{CC} Read Energy Consumption (Watt/Sec)	5.0V V_{CC} Read Energy Compared to the 28F016XS	3.3V V_{CC} Read Energy Consumption (Watt/Sec)	3.3V V_{CC} Read Energy Compared to the 28F016XS
28F016XS Flash Memory (x16)	6.7×10^{-6}	1x	3.2×10^{-6}	1x
16-Mbit DRAM (x16)	9.2×10^{-6}	1.4x	4.6×10^{-6}	1.4x
4-Mbit SRAM (two x8)	38×10^{-6}	5.7x	40×10^{-6}	12.5x
1-Mbit Cache SRAM (two x8)	17×10^{-6}	2.5x	10×10^{-6}	3.1x
16-Mbit Paged Mask ROM (x16)	6.8×10^{-6}	1.01x	4.8×10^{-6}	1.5x
4-Mbit EPROM (x16)	9.6×10^{-6}	1.4x	7.1×10^{-6}	2.2x
1-Mbit EEPROM (x16)	15×10^{-6}	2.2x	14×10^{-6}	4.4x
1.8" HDD	57.8×10^{-3}	>>	N/A	N/A
1.3" HDD	23.5×10^{-3}	>>	N/A	N/A

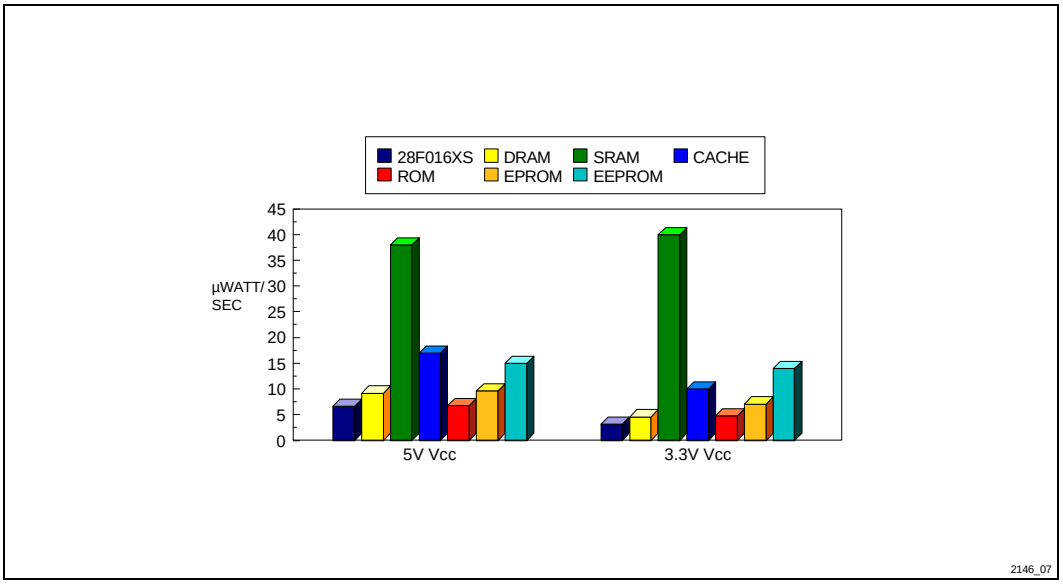

Figure 7. The 28F016XS's Low Power/High Performance Combination Result in the Lowest Read Energy of Any Memory Technology

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Standby Power Consumption

The 28F016XS's standby power is much lower than that of any other updateable memory and compares favorably with that of EPROM and mask ROM. DRAM refresh requirements cause their true standby power consumption to be a combination of the "datasheet" standby power and much larger refresh power. The calculations that follow also do not include the power consumption of the DRAM controller refresh circuitry, which would result in even larger effective DRAM subsystem power draw. Figure 8 does not show cache SRAM and HDD due to their very high standby power consumption specifications.

Table 3. Standby Power Consumption Comparisons

Memory Technology	5.0V V_{CC} Standby Power Consumption (Watt)	5.0V V_{CC} Standby Power Compared to the 28F016XS	3.3V V_{CC} Standby Power Consumption (Watt)	3.3V V_{CC} Standby Power Compared to the 28F016XS
28F016XS Flash Memory (x16)	650×10^{-6}	1x	429×10^{-6}	1x
16-Mbit DRAM (x16)	50×10^{-3}	76.9x	26.4×10^{-3}	61.5x
4-Mbit SRAM (two x8)	1×10^{-3}	1.5x	528×10^{-6}	1.2x
1-Mbit Cache SRAM (two x8)	400×10^{-3}	615x	198×10^{-3}	461.5x
16-Mbit Paged Mask ROM (x16)	500×10^{-6}	0.8x	330×10^{-6}	0.8x
4-Mbit EPROM (x16)	500×10^{-6}	0.8x	330×10^{-6}	0.8x
1-Mbit EEPROM (x16)	2.5×10^{-3}	3.9x	990×10^{-6}	2.3x
1.8" HDD	750×10^{-3}	1153.9x	N/A	N/A
1.3" HDD	500×10^{-3}	769.2x	N/A	N/A

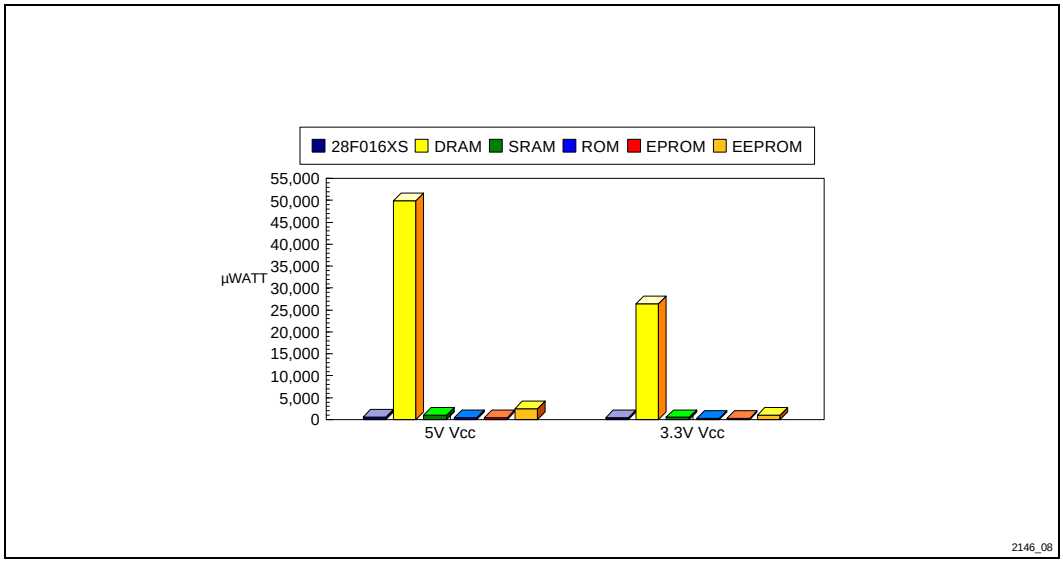

Figure 8. DRAM Refresh Requirements Significantly Impact Standby Power Consumption

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Sleep Power Consumption

The 28F016XS, DRAM and HDD are the only memory technologies that offer a distinct sleep mode with lower power consumption compared to standby. The 28F016XS in deep power-down mode has much lower power consumption than all other memories. DRAM still requires refresh (the internal self-refresh operation). The HDD motor is no longer spinning, but control circuitry continues to draw power. Figure 9 does not include cache RAM or HDD due to their very high sleep power consumption specifications.

Table 4. Sleep Power Consumption Comparisons

Memory Technology	5.0V V_{CC} Sleep Power Consumption (Watt)	5.0V V_{CC} Sleep Power Compared to the 28F016XS	3.3V V_{CC} Sleep Power Consumption (Watt)	3.3V V_{CC} Sleep Power Compared to the 28F016XS
28F016XS Flash Memory (x16)	25×10^{-6}	1x	16.5×10^{-6}	1x
16-Mbit DRAM (x16)	2×10^{-3}	80x	990×10^{-6}	60x
4-Mbit SRAM (two x8)	1×10^{-3}	40x	528×10^{-6}	32x
1-Mbit Cache SRAM (two x8)	400×10^{-3}	16,000x	198×10^{-3}	12,000x
16-Mbit Paged Mask ROM (x16)	500×10^{-6}	20x	330×10^{-6}	20x
4-Mbit EPROM (x16)	500×10^{-6}	20x	330×10^{-6}	20x
1-Mbit EEPROM (x16)	2.5×10^{-3}	100x	990×10^{-6}	60x
1.8" HDD	25×10^{-3}	1000x	N/A	N/A
1.3" HDD	15×10^{-3}	600x	N/A	N/A

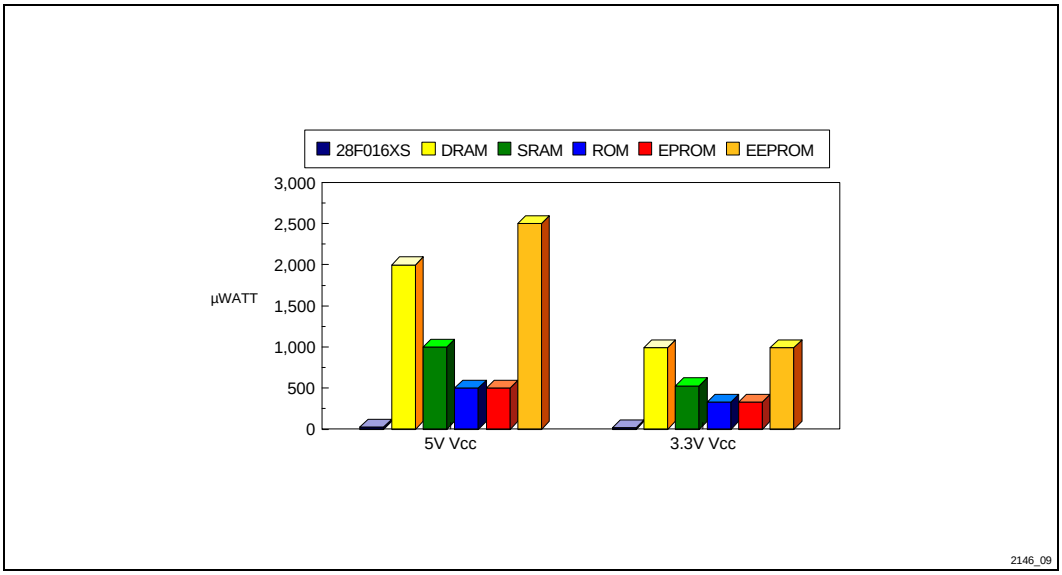

Figure 9. The 28F016XS's Deep Power-Down Mode Results in Extremely Low Sleep Power Consumption

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3.0 THE 28F016XS-BASED MEMORY ARCHITECTURE AND ITS POSITIVE SYSTEM IMPACTS

3.1 The Traditional Memory Model Has a Long History

The memory architecture shown in Figure 4, with only minor variation, has appeared for decades in almost every area of computing. This model consists of four basic parts:

- SRAM cache memory (very fast, very expensive, low density, volatile)
- DRAM main memory (moderately fast, moderately expensive, moderate density, volatile)
- ROM boot memory (moderately slow, moderately cheap, low or high density, nonvolatile)
- Magnetic media archive memory (very slow, very cheap, high density, nonvolatile)

Cost-per-bit fundamentally determines the percentage of total system memory budget devoted to each memory type. SRAM delivers very fast reads and writes but achieves this performance through cell and manufacturing process complexity, which impacts cost and density. On the other end of the spectrum, magnetic media gives lower performance but provides very low media cost. Varying amounts of each memory type combine in a computer system to meet price and performance expectations. Many of today's mainstream desktop PCs, for example, contain a 256-Kbyte cache and a 540-Mbyte HDD, a ratio of almost 1:2,000!

Volatility provides another important consideration when choosing memories. Volatile memories (RAM) historically have provided higher performance, but lose all data when power is removed. They therefore, must remain powered-up the entire time the system is operational. DRAM additionally must be refreshed periodically to preserve stored data. Lower-performance, nonvolatile memories (ROM and magnetic media) retain their contents on power loss, and are needed in a computer to store the operating software between uses.

ROM gives faster read performance than magnetic media (although slower than RAM), but its contents cannot be changed once stored. Systems that contain a relatively small amount of resident code (several megabytes) often keep it in ROM. As resident software size grows, code stability becomes a significantly greater concern. As a result, in these systems ROM often contains only a small kernel of system boot code that will, hopefully, remain usable over the life of the system. The vast majority of software resides on slower, updateable magnetic media. Regardless of the nonvolatile memory chosen, the system copies code and files to DRAM for execution, and the most-commonly accessed data and code execute out of the fast SRAM cache (see Figure 10).

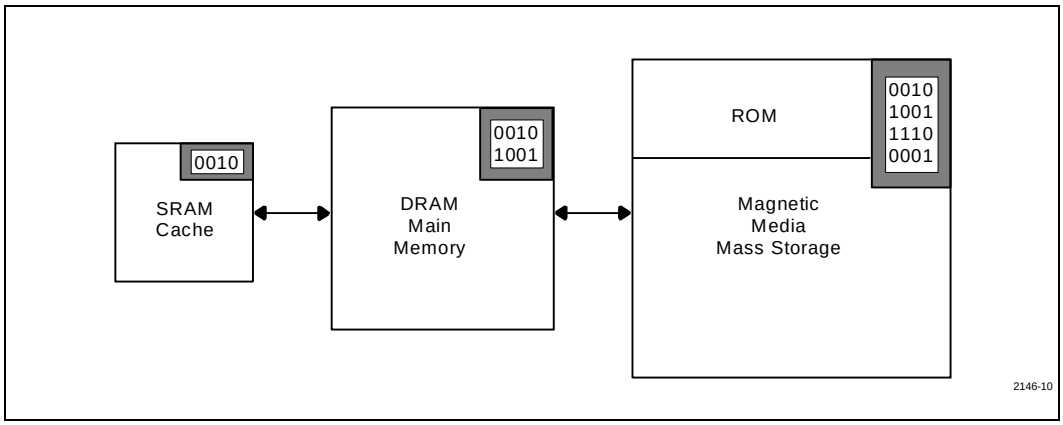

Figure 10. Redundant Memory Stores Common Code and Data in Multiple Locations

The staying power of the traditional memory model is impressive, given the blistering pace and rigorous requirements of the electronics industry. In fact, it is precisely the evolution and innovation of memory technology that has ensured the continued domination of traditional memory types in everything from mainframes to mobile computers to embedded computing systems of all types. However, as microprocessor performance accelerates exponentially and emerging computing models make stringent new demands, the traditional memory model is being challenged.

3.2 The Traditional Memory Model Hits a Brick Wall

Users expect next-generation computing systems to improve performance and add features while simultaneously lowering cost, minimizing power consumption, increasing reliability and shrinking form factor and weight. The traditional memory model was not intended for systems with these constraints, and continued innovation within this model produce diminishing returns.

Poor System Performance

The performance of the traditional memory hierarchy (where software is copied from nonvolatile media to DRAM and then to SRAM) doesn't optimize the performance of today's fast microprocessors, especially when performance is measured in MIPS-per-watt rather than raw MIPS. Both system boot time and application task switching response slow down because of NVM-to-RAM file load delays, and disk drive spin-up time hinders recovery time from system power savings modes to full operation. Even assuming an aggressive HDD-to-DRAM transfer rate, operating system load delays can take many seconds (or tens or seconds), before execution out of DRAM even begins!

Redundant Memory Cost

Component cost alone does not provide adequate criteria for selecting the proper memory subsystem. Memory selection requires first identifying the key-user requirements that the system must satisfy, and then choosing the memory technology that meets or exceeds these requirements at the lowest cost. Unnecessary memory duplication translates to unnecessary additional system cost. When evaluating memory subsystem cost alternatives, remember to include ALL memory in calculations (i.e., not only HDD and/or ROM but also DRAM and SRAM) plus any system control logic needed to interface to the memory.

Short Battery Life

DRAMs must be constantly refreshed by the memory controller to preserve their stored data. The HDD draws current with every motor rotation and may actually draw more average current if it is "parked" too frequently, since spin-up causes high current draw. As the power draw of other computer subsystems (CPU, screen, etc.) drops with continued innovation, memory subsystem power consumption becomes a greater percentage of the total system drain and significantly impacts battery life.

Low Reliability and Unacceptable Ruggedness

Magnetic media alternatives (floppy disk drive, hard disk drive, etc.) contain moving parts, relatively fragile media and narrow operating temperature ranges. These products, though improving, have unacceptably low tolerance to shock, vibration and movement during read/write. A mass storage approach based on a disk rotating at high RPM with a read/write head micrometers above it, capable of colliding at the slightest shock and permanently destroying data, is fundamentally incompatible with the vision of a fully-mobile computing machine.

Multiple levels of memory mean multiple levels of potential component failure. Excessive heat generation also impacts system lifetime, and the large number of board traces required is a significant manufacturing challenge and reliability headache.

Large Form Factor and Excessive Weight

The traditional memory model contains unnecessary memory duplication. A large portion of DRAM in the system is used only to provide the CPU with access to programs that already exist on ROM or the hard disk or floppy drive. The traditional memory model needs redundant DRAM and magnetic media or ROM because DRAM satisfies the performance needs of the processor while ROM or HDD provides the nonvolatility the system requires. This duplication takes up excessive space within the system, impacting its footprint and thickness. The added power consumption requires larger system batteries and power supplies, which make the system unacceptably and unnecessarily heavy.

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3.3 The 28F016XS Flash Memory Architecture Alternative

Just as today's system designs are revolutionary, so too are their memory architectures. Incremental improvements to the traditional approach no longer measure up to the revolutionary potential of a 28F016XS-based alternative (see Figure 5).

Optimized System Performance

The 28F016XS provides both high performance, like DRAM and SRAM, and non-volatility, like ROM and HHD. It combines the best qualities of both memory types in one technology. Lengthy software load overhead and task switching delays are eliminated. Code runs as fast or faster than that in DRAM with much less system hardware complexity, and the 28F016XS read transfer rate approaches that of cache SRAM!

Low Cost and Flexible

A 28F016XS flash memory array is competitively priced to a DRAM/ROM or DRAM/small HDD combination, especially when the costs of associated memory interface and control circuitry are considered. Unlike ROM, flash memory is in-system updateable. This allows easy code upgrade even after the system is in a customer's hands, to enhance capabilities or correct unintended system shortcomings. This flexibility keeps system costs low both initially and throughout system lifetime.

Minimal Power Consumption

Flash memory, being nonvolatile, requires no periodic refresh and no constant power to be applied to it in order to retain stored information. The 28F016XS's read energy is the lowest of any memory technology analyzed in this application note. The 28F016XS's standby and sleep power also compare very favorably with alternative approaches. The redundancy of multiple memory technologies in the traditional memory architecture results in multiple sources of power consumption. These multiple memories must be summed to determine the true memory subsystem power draw. With the 28F016XS, there is only one very efficient memory technology, consuming very little system power.

High Reliability, Solid-State Ruggedness

Solid-state memories such as the 28F016XS are inherently more rugged and shock-resistant than alternatives containing moving parts, like HDDs. The 28F016XS-based memory architecture, being simpler and more integrated than the traditional alternative, also exhibits much higher system reliability. Data reliability studies point to the longevity of data stored in flash memory.

Small Form Factor, Light Weight

The 28F016XS's compact TSOP package provides 9.2 Mbyte/in^2 density capability, with components mounted on both sides of the system board. The 28F016XS memory subsystem architecture minimizes or eliminates memory duplication, leading to substantial board space savings. The 28F016XS's very low power consumption reduces the size and weight of system batteries and power supplies.

4.0 CONCLUSION

This application note has discussed performance and power/energy comparisons between the 28F016XS and other memory technologies, and the positive 28F016XS impacts on system performance and power consumption. Consult reference documentation for a more complete understanding of device capabilities and design techniques. Please contact your local Intel or distribution sales office for more information on Intel's flash memory products.

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ADDITIONAL INFORMATION

Order Number	Document/Tool
290532	28F016XS 16-Mbit (1 Mbit x 16, 2 Mbit x 8) Synchronous Flash Memory Datasheet
297500	“Interfacing the 28F016XS to the i960 ® Microprocessor Family” (Technical Paper)
297504	“Interfacing the 28F016XS to the Intel486™ Microprocessor Family” (Technical Paper)
292147	AP-398,“Designing with the 28F016XS”
292163	AP-610, “Flash Memory In-System Code and Data Update Techniques”
292165	AB-62, “Compiled Code Optimizations for Embedded Flash RAM Memories”
297372	16-Mbit Flash Product Family User’s Manual
297508	FLASHBuilder Utility
Contact Intel/Distribution Sales Office	28F016XS Benchmark Utility
Contact Intel/Distribution Sales Office	28F016XS iBIS Models
Contact Intel/Distribution Sales Office	28F016XS VHDL/Verilog Models
Contact Intel/Distribution Sales Office	28F016XS Timing Designer Library Files
Contact Intel/Distribution Sales Office	28F016XS Orcad and ViewLogic Schematic Symbols

REVISION HISTORY

Number	Description
001	Original Version
002	Minor text edits related to 28F016XS feature set change: -Page Buffer functionality removed -RY/BY# reconfiguration removed -Erase All Unlocked Blocks, Two-Byte Write command removed -Software Sleep Abort removed -Command queuing capability removed

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APPENDIX A

28F016XS FLASH MEMORY

The following sections provide detailed analysis of the memory performance and power/energy consumption comparisons discussed in Section 2.0 of this application note.

Read Performance (5.0V V_{CC})

The 28F016XS-15 is capable of 3-1-1-1-1-1-1-1.... read performance at 5.0V V_{CC} and 33 MHz (2-0-0-0-0-0-0-0.... in terms of wait-states). This results in a 66.1 Mbyte/sec read transfer rate, as shown by the calculation below:

512 bytes/(258 clocks x 30 ns/clock) = x Mbyte/sec
x = 66.1 Mbyte/sec

Read Performance (3.3V V_{CC})

The 28F016XS-15 is capable of 3-1-2-1-2-1-2-1.... read performance at 3.3V V_{CC} and 33 MHz (2-0-1-0-1-0-1-0.... in terms of wait-states). This results in a 44.3 Mbyte/sec read transfer rate, as shown by the calculation below:

512 bytes/(385 clocks x 30 ns/clock) = x Mbyte/sec
x = 44.3 Mbyte/sec

Power and Energy Consumption (5.0V V_{CC})

Read mode power consumption is 875 mW (5.0V x 175 mA). Read mode energy consumption is 6.7 µJoules (875 mW x 258 clocks x 30 ns/clock).

Standby power consumption is 650 µW (5.0V x 130 µA). Deep power-down (sleep) power consumption is 25 µW (5.0V x 5 µA).

Power and Energy Consumption (3.3V V_{CC})

Read mode power consumption is 280 mW (3.3V x 85 mA). Read mode energy consumption is 3.2 µJoules (280 mW x 385 clocks x 30 ns/clock).

Standby power consumption is 429 µW (3.3V x 130 µA). Deep power-down (sleep) power consumption is 16.5 µW (3.3V x 5 µA).

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16-Mbit DRAM

16-Mbit DRAMs were, at the time this application note was published, only beginning to ramp into production. Only advance information for the wider x16 16-Mbit DRAMs was available for use in the calculations that follow.

Read Performance (5.0V V_{CC} and 3.3V V_{CC})

Sequential reads allow use of the DRAM fast page mode. Assumed DRAM specifications are shown below:

- 70 ns t_{RAC}, 35 ns t_{AA} (5.0V V_{CC})
- 80 ns t_{RAC}, 45 ns t_{AA} (3.3V V_{CC})
- 256-word (512-byte) page buffer

Therefore, 16-Mbit DRAMs are capable of 3-2-2-2-2-2-2-2.... read performance at 33 MHz (2-1-1-1-1-1-1-1 in terms of wait-states....). This results in a 33.3 Mbyte/sec read transfer rate, as shown by the calculation below:

512 bytes/(513 clocks x 30 ns/clock) = x Mbyte/sec
x = 33.3 Mbyte/sec

Power and Energy Consumption (5.0V V_{CC})

Read mode power consumption is 600 mW (5.0V x 120 mA). Read mode energy consumption is 9.2 µJoules (600 mW x 513 clocks x 30 ns/clock).

The standby mode power calculation combines both the DRAM standby current and refresh current specifications, in proportion relative to percentage of time in each mode. Standby power consumption is 50 mW (5.0V x 10 mA). Sleep power calculations use the DRAM self-refresh current specification. Sleep power consumption is 2 mW (5.0V x 400 µA).

Power and Energy Consumption (3.3V V_{CC})

Read mode power consumption is 297 mW (3.3V x 90 mA). Read mode energy consumption is 4.6 µJoules (297 mW x 513 clocks x 30 ns/clock).

Standby power consumption is 26.4 mW (3.3V x 8 mA). Sleep power consumption is 990 µW (3.3V x 300 µA).

4-Mbit SRAM

4-Mbit SRAMs were, at the time this application note was published, only beginning to ramp into production. Only advance information for the wide x8 4-Mbit SRAMs was available for use in the calculations that follow. This analysis used two 4-Mbit (x8) SRAMs to create the assumed 16-bit system interface.

Read Performance (5.0V V_{CC})

The assumed 5.0V V_{CC} 4-Mbit SRAM access time is 55 ns. Therefore, 4-Mbit SRAMs are capable of 2-2-2-2-2-2-2-2.... read performance at 5.0V V_{CC} and 33 MHz (1-1-1-1-1-1-1-1.... in terms of wait-states). This results in a 33.3 Mbyte/sec read transfer rate, as shown by the calculation below:

512 bytes/(512 clocks x 30 ns/clock) = x Mbyte/sec
x = 33.3 Mbyte/sec

Read Performance (3.3V V_{CC})

The assumed 3.3V V_{CC} 4-Mbit SRAM access time is 100 ns. Therefore, 4-Mbit SRAMs are capable of 4-4-4-4-4-4-4-4.... read performance at 3.3V V_{CC} and 33 MHz (3-3-3-3-3-3-3-3.... in terms of wait-states). This results in a 16.7 Mbyte/sec read transfer rate, as shown by the calculation below:

512 bytes/(1024 clocks x 30 ns/clock) = x Mbyte/sec
x = 16.7 Mbyte/sec

Power and Energy Consumption (5.0V V_{CC})

Read mode power consumption is 2.5W (5.0V x 250 mA x 2 devices). Read mode energy consumption is 38 µJoules (2.5W x 512 clocks x 30 ns/clock).

Standby power consumption is 1 mW (5.0V x 100 µA x 2 devices). Data retention current at 5.0V V_{CC} is the same as standby current, therefore data retention (sleep) power consumption is 1 mW.

Power and Energy Consumption (3.3V V_{CC})

Read mode power consumption is 1.3W (3.3V x 200 mA x 2 devices). Read mode energy consumption is 40 µJoules (1.3W x 1024 clocks x 30 ns/clock).

Standby power consumption is 528 µW (3.3V x 80 µA x 2 devices). Data retention current at 3.3V V_{CC} is the same as standby current, therefore data retention (sleep) power consumption is 528 µW.

ADVANCE INFORMATION

1-Mbit CACHE SRAM

The majority of memories analyzed in this application note were high density. 1-Mbit cache SRAMs were included, however, to compare the read performance and power/energy consumption of 28F016XS with that of L2 cache memory. This analysis used two 1-Mbit (x8) cache SRAMs to create the assumed 16-bit system interface.

Read Performance (5.0V V_{CC} and 3.3V V_{CC})

Assumed 1-Mbit cache SRAM specifications are shown below:

- 15 ns t_{ACC} (5.0V V_{CC})
- 20 ns t_{ACC} (3.3V V_{CC})

Therefore, 1-Mbit cache SRAMs are capable of 1-1-1-1-1-1-1-1.... read performance at 33 MHz (0-0-0-0-0-0-0-0.... in terms of wait-states). This results in a 66.7 Mbyte/sec read transfer rate, as shown by the calculation below:

512 bytes/(256 clocks x 30 ns/clock) = x Mbyte/sec
x = 66.7 Mbyte/sec

Power and Energy Consumption (5.0V V_{CC})

Read mode power consumption is 2.2W (5.0V x 220 mA x 2 devices). Read mode energy consumption is 17 µJoules (2.2W x 256 clocks x 30 ns/clock).

Standby power consumption is 400 mW (5.0V x 40 mA x 2 devices). Data retention current at 5.0V V_{CC} is the same as standby current, therefore data retention (sleep) power consumption is 400 mW.

Power and Energy Consumption (3.3V V_{CC})

Read mode power consumption is 1.3W (3.3V x 200 mA x 2 devices). Read mode energy consumption is 10 µJoules (1.3W x 256 clocks x 30 ns/clock).

Standby power consumption is 198 mW (3.3V x 30 mA x 2 devices). Data retention current at 3.3V V_{CC} is the same as standby current, therefore data retention (sleep) power consumption is 198 mW.

ADVANCE INFORMATION

16-Mbit PAGED MASK ROM

Calculations that follow used the x16 version of the 16-Mbit paged mask ROM, which is not yet widely available from multiple vendors. The x8 16-Mbit paged mask ROM is the more common version today.

Read Performance (5.0V V_{CC})

Sequential reads allow use of the mask ROM page mode. The assumed 5.0V V_{CC} 16-Mbit mask ROM random access time is 150 ns, with 75 ns accesses in page mode (4-word page). Therefore, 16-Mbit mask ROMs are capable of 5-3-3-3-5-3-3-3.... read performance at 5.0V V_{CC} and 33 MHz (4-2-2-2-4-2-2-2.... in terms of wait-states). This results in a 19 Mbyte/sec read transfer rate, as shown by the calculation below:

12 bytes/(900 clocks x 30 ns/clock) = x Mbyte/sec
x = 19 Mbyte/sec

Read Performance (3.3V V_{CC})

The assumed 3.3V V_{CC} 16-Mbit mask ROM random access time is 200 ns, with 100 ns accesses in page mode (4-word page). Therefore, 16-Mbit mask ROMs are capable of 7-4-4-4-7-4-4-4.... read performance at 3.3V V_{CC} and 33 MHz (6-3-3-3-6-3-3-3.... in terms of wait-states). This results in a 14 Mbyte/sec read transfer rate, as shown by the calculation below:

512 bytes/(1216 clocks x 30 ns/clock) = x Mbyte/sec
x = 14 Mbyte/sec

Power and Energy Consumption (5.0V V_{CC})

Read mode power consumption is 250 mW (5.0V x 50 mA). Read mode energy consumption is 6.8 µJoules (250 mW x 900 clocks x 30 ns/clock).

Standby power consumption is 500 µW (5.0V x 100 µA). 16-Mbit mask ROM does not provide a sleep mode, so sleep current is equal to standby current, or 500 µW.

Power and Energy Consumption (3.3V V_{CC})

Read mode power consumption is 132 mW (3.3V x 40 mA). Read mode energy consumption is 4.8 µJoules (132 mW x 1216 clocks x 30 ns/clock).

Standby power consumption is 330 µW (3.3V x 100 µA). 16-Mbit mask ROM does not provide a sleep mode, so sleep current is equal to standby current, or 330 µW.

ADVANCE INFORMATION

4-Mbit EPROM

Calculations that follow used the x16 version of the 4-Mbit EPROM (Intel 27C400 or equivalent).

Read Performance (5.0V V_{CC})

The assumed 5.0V V_{CC} 4-Mbit EPROM random access time is 150 ns. Therefore, 4-Mbit EPROMs are capable of 5-5-5-5-5-5-5-5.... read performance at 5.0V V_{CC} and 33 MHz (4-4-4-4-4-4-4-4.... in terms of wait-states). This results in a 13.3 Mbyte/sec read transfer rate, as shown by the calculation below:

512 bytes/(1280 clocks x 30 ns/clock) = x Mbyte/sec
x = 13.3 Mbyte/sec

Read Performance (3.3V V_{CC})

The assumed 3.3V V_{CC} 4-Mbit EPROM random access time is 200 ns. Therefore, 4-Mbit EPROMs are capable of 7-7-7-7-7-7-7-7.... read performance at 3.3V V_{CC} and 33 MHz (6-6-6-6-6-6-6-6.... in terms of wait-states). This results in a 9.5 Mbyte/sec read transfer rate, as shown by the calculation below:

512 bytes/(1792 clocks x 30 ns/clock) = x Mbyte/sec
x = 9.5 Mbyte/sec

Power and Energy Consumption (5.0V V_{CC})

Read mode power consumption is 250 mW (5.0V x 50 mA). Read mode energy consumption is 9.6 µJoules (250 mW x 1280 clocks x 30 ns/clock).

Standby power consumption is 500 µW (5.0V x 100 µA). 4-Mbit EPROM does not provide a sleep mode, so sleep current is equal to standby current, or 500 µW.

Power and Energy Consumption (3.3V V_{CC})

Read mode power consumption is 132 mW (3.3V x 40 mA). Read mode energy consumption is 7.1 µJoules (132 mW x 1792 clocks x 30 ns/clock).

Standby power consumption is 330 µW (3.3V x 100 µA). 4-Mbit EPROM does not provide a sleep mode, so sleep current is equal to standby current, or 330 µW.

1-Mbit EEPROM

This analysis used two 1-Mbit (x8) EEPROMs to create the assumed 16-bit system interface.

Read Performance (5.0V V_{CC})

The assumed 5.0V V_{CC} 1- Mbit EEPROM random access time is 120 ns. Therefore, 1-Mbit EEPROMs are capable of 4-4-4-4-4-4-4-4.... read performance at 5.0V V_{CC} and 33 MHz (3-3-3-3-3-3-3-3.... in terms of wait-states). This results in a 16.7 Mbyte/sec read transfer rate, as shown by the calculation below:

512 bytes/(1024 clocks x 30 ns/clock) = x Mbyte/sec
x = 16.7 Mbyte/sec

Read Performance (3.3V V_{CC})

The assumed 3.3V V_{CC} 1-Mbit EEPROM random access time is 200 ns. Therefore, 1-Mbit EEPROMs are capable of 7-7-7-7-7-7-7-7.... read performance at 3.3V V_{CC} and 33 MHz (6-6-6-6-6-6-6-6.... in terms of wait-states). This results in a 9.5 Mbyte/sec read transfer rate, as shown by the calculation below:

512 bytes/(1792 clocks x 30 ns/clock) = x Mbyte/sec
x = 9.5 Mbyte/sec

Power and Energy Consumption (5.0V V_{CC})

Read mode power consumption is 500 mW (5.0V x 100 mA). Read mode energy consumption is 15 µJoules (500 mW x 1024 clocks x 30 ns/clock).

Standby power consumption is 2.5 mW (5.0V x 500 µA). 1- Mbit EEPROM does not provide a sleep mode, so sleep current is equal to standby current, or 2.5 mW.

Power and Energy Consumption (3.3V V_{CC})

Read mode power consumption is 264 mW (3.3V x 80 mA). Read mode energy consumption is 14 µJoules (264 mW x 1792 clocks x 30 ns/clock).

Standby power consumption is 990 µW (3.3V x 300 µA). 1-Mbit EEPROM does not provide a sleep mode, so sleep current is equal to standby current, or 990 µW.

ADVANCE INFORMATION

1.8" HDD

Only information for 5.0V V_{CC} 1.8" HDDs was used in the calculations that follow; 3.3V V_{CC} 1.8" HDDs were not yet available.

Read Performance (5.0V V_{CC})

The HDD must first locate data stored on its platter(s) and transfer it to the sector buffer before the system can read it. The assumed 5.0V V_{CC} 1.8" HDD seek access time (including rotational latency) is 30 ms. The assumed peak media transfer rate is 2 Mbyte/sec or 477 ns/byte, and the peak interface transfer rate is 3 Mbyte/sec or 318 ns/byte. Therefore, 1.8" HDD at 5.0V V_{CC} can access 256 words (512 bytes) of data in 30.4 ms (1 x 10^6 33 MHz clocks), resulting in a 16.8 Kbyte/sec read transfer rate, as shown by the calculations below:

Access time = 30 ms + (477 ns/byte x 512 bytes) + (318 ns/byte x 512 bytes) = 30.4 ms (1 clock/30 ns) x (30.4 ms) = 1 x 10^6 33 MHz clocks 512 bytes/30.4 ms = x Mbyte/sec x = 16.8 Kbyte/sec

Effective read transfer rate is highly dependent on length of read sequence.

Power and Energy Consumption (5.0V V_{CC})

Read mode power consumption is 1.9 W (5.0V x 380 mA). Read mode energy consumption is 57.8 mJoules ((1.9 W) x (1 x 10^6 clocks) x (30 ns/clock)).

Standby power consumption is 750 mW (5.0V x 150 mA). Sleep power consumption is 25 mW (5.0V x 5 mA).

1.3" HDD

Only information for 5.0V V_{CC} 1.3" HDDs was used in the calculations that follow; 3.3V V_{CC} 1.3" HDDs were not yet available.

Read Performance (5.0V V_{CC})

The HDD must first locate data stored on its platter(s) and transfer it to the sector buffer before the system can read it. The assumed 5.0V V_{CC} 1.3" HDD seek access time (including rotational latency) is 15 ms. The assumed peak media transfer rate is 1.5 Mbyte/sec or 636 ns/byte, and the peak interface transfer rate is also 1.5 Mbyte/sec or 636 ns/byte. Therefore, 1.3" HDD at 5.0V V_{CC} can access 256 words (512 bytes) of data in 15.7 ms (522 x 10^3 33 MHz clocks), resulting in a 32.7 Kbyte/sec read transfer rate, as shown by the calculations below:

Access time = 15 ms + (636 ns/byte x 512 bytes) + (636 ns/byte x 512 bytes) = 15.7 ms (1 clock/30 ns) x (15.7 ms) = 522 x 10^3 33 MHz clocks 512 bytes/ 15.7 ms = x Mbyte/secx = 32.7 Kbyte/sec

Effective read transfer rate is highly dependent on length of read sequence.

Power and Energy Consumption (5.0V V_{CC})

Read mode power consumption is 1.5 W (5.0V x 300 mA). Read mode energy consumption is 23.5 mJoules ((1.5 W) x (522 x 10^3 clocks) x (30 ns/clock)).

Standby power consumption is 500 mW (5.0V x 100 mA). Sleep power consumption is 15 mW (5V x 3 mA).

ADVANCE INFORMATION