AP-393

APPLICATION NOTE

28F016SV Compatibility with 28F016SA

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1.0 INTRODUCTION

This application note discusses compatibility between the 28F016SV and 28F016SA FlashFile™ memory components. It also offers recommendations for designing systems using the 28F016SA today, when future conversion to the 28F016SV is planned.

The 28F016SV is a member of Intel's second-generation 16-Mbit FlashFile component product family. It improves upon the 28F016SA in the following areas:

- SmartVoltage technology
  - — Selectable 5.0V or 12.0V V_{PP}
- Faster read performance
- Higher Page Buffer write performance at 12.0V V_{PP}
- Enhanced device feedback after writing the Upload Device Information command
- Additional RY/BY# configuration
  - — Pulse-On-Write/Erase

2.0 COMPATIBILITY

The 28F016SV and 28F016SA are both manufactured on Intel's fourth-generation 0.6 micron ETOX™ IV process technology. This technology enables random access flash memory products with the highest read/write performance and lowest power consumption. ETOX flash memory technology also achieves very high quality and reliability.

The following sections discuss specific areas of compatibility between the 28F016SV and the 28F016SA. Please reference the documentation listed in the Additional Information section of this application note for a full description of these flash memory components.

2.1 Pinout and Package

The 28F016SV is fully pinout backwards-compatible with the 28F016SA (see Figures 1 and 2). Both devices are available in 56-lead TSOP and SSOP packages.

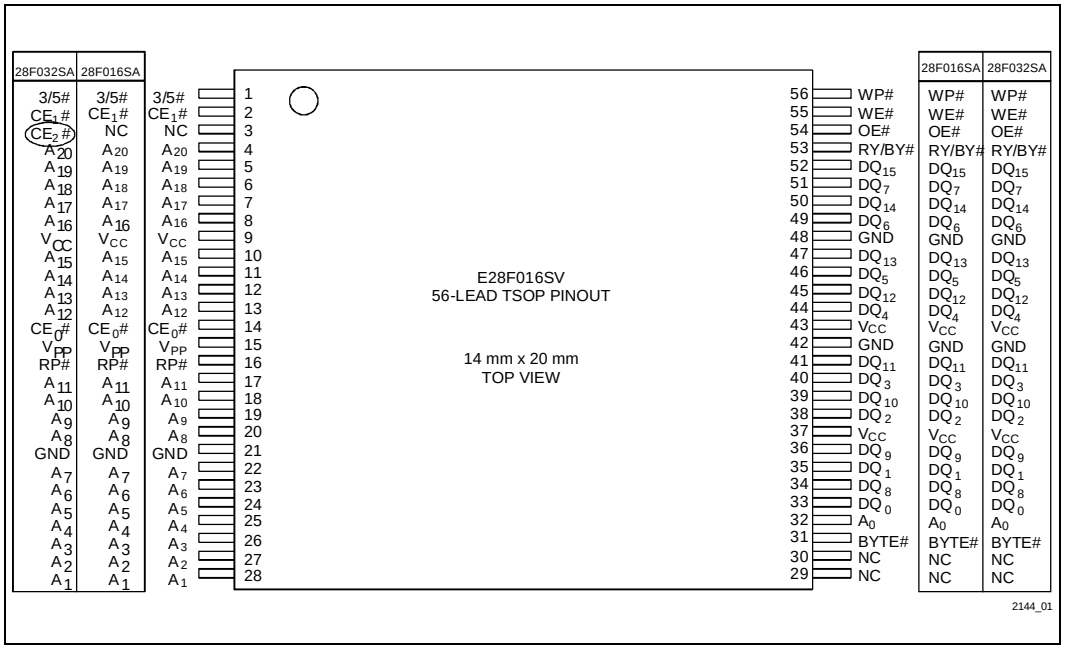

Figure 1. 28F016SV 56-Lead TSOP Pinout Compared to the 28F016SA and 28F032SA

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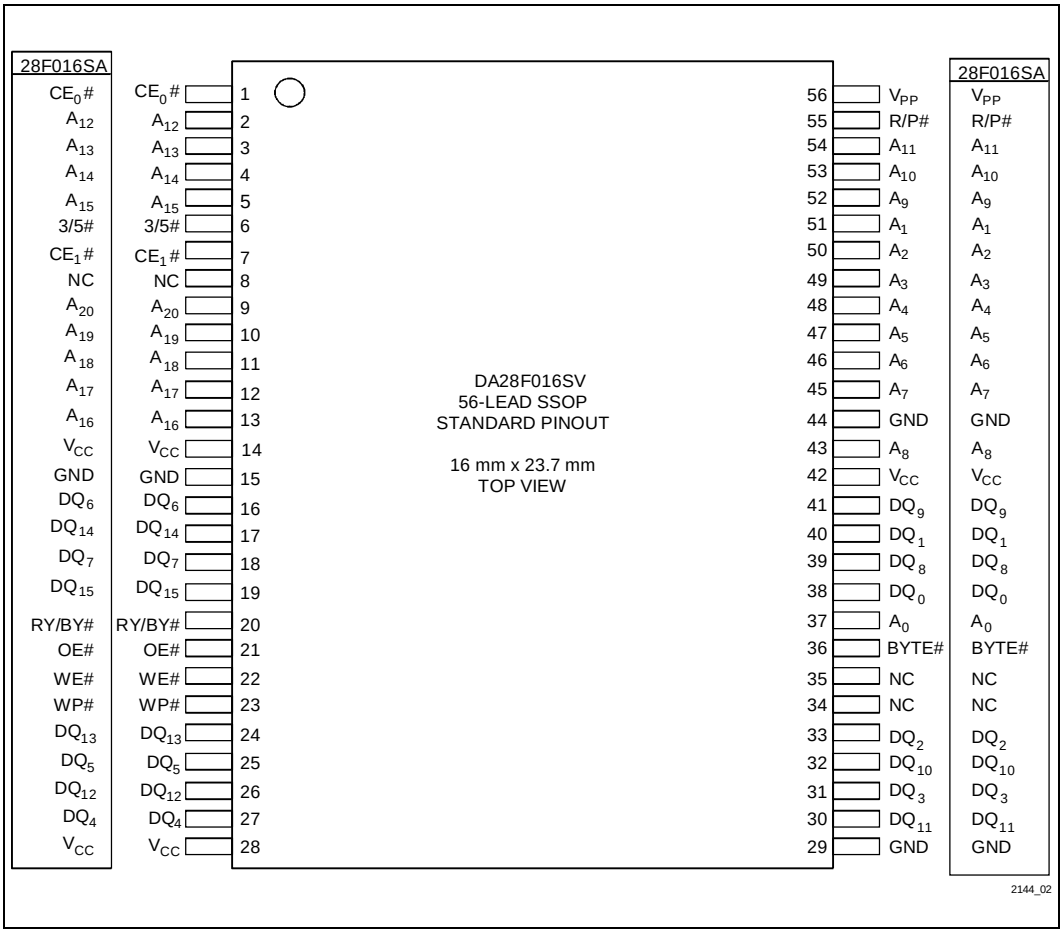

Figure 2. 28F016SV 56-Lead SSOP Pinout Compared to the 28F016SA

2.2 Bus Operations

The 28F016SV shares the same bus operations as the 28F016SA, and both flash memories operate identically in these operating modes.

2.3 Command Definitions

The 28F016SV shares the same command set as the 28F016SA. All commands produce compatible internal operations for both flash memories.

The 28F016SV includes an additional RY/BY# mode, RY/BY# Pulse on Write/Erase, enabled as part of the RY/BY# Configuration (96H) command sequence. This mode was “reserved for future use” on the 28F016SA.

The 28F016SV also enhances the device feedback after writing the Upload Device Information (99H) command sequence. It outputs not only the Device Revision Number (compatible with the 28F016SA), but the Device Proliferation Code and Device Configuration Code. See Section 2.5 for more information on these topics.

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2.4 Status Registers

The 28F016SV and 28F016SA both have a Compatible Status Register (CSR), Global Status Register (GSR) and 32 Block Status Registers (BSRs). Register address maps for both flash memories are identical.

Compatible Status Register

CSR bits 4–7 have identical functions for both the 28F016SV and the 28F016SA. CSR bits 0–2 are marked "reserved for future use" for both the 28F016SV and 28F016SA.

CSR bit 3 (V_{PP} Status) has been functionally enhanced on the 28F016SV, reflective of the ability to Data Write and Erase with V_{PP} = 5.0V ± 10% (V_{PPH1}) or V_{PP} = 12.0V ± 5% (V_{PPH2}). See Section 2.7 for more information on 28F016SV Data Write and Erase. CSR.3 = "1" is defined as "V_{PP} Error" on the 28F016SV, versus "V_{PP} Low" on the 28F016SA. If Data Write or Erase is initiated with V_{PP} = V_{PPH2}, subsequent V_{PP} transitions above V_{PPH2}(max) or below V_{PPH2}(min) will, if detected, terminate the operation in progress and set CSR.3 to "1" (this functionality matches the 28F016SA). Additionally, if Data Write or Erase is initiated with V_{PP} = V_{PPH1}, subsequent V_{PP} transitions above V_{PPH1}(max) or below V_{PPH1}(min) will, if detected, also terminate the operation in progress and set CSR.3 to "1." See Table 1 for the 28F016SV's Compatibile Status Register.

Global Status Register

All GSR bits have identical functions for both the 28F016SV and the 28F016SA.

Block Status Registers

BSR bits 3–7 have identical functions for both the 28F016SV and the 28F016SA. BSR bit 0 is marked "reserved for future use" for both the 28F016SV and the 28F016SA.

BSR bit 2 (V_{PP} Status) has been functionally enhanced on the 28F016SV compared to the 28F016SA. See the earlier description of CSR.3 for more information.

BSR bit 1, marked "reserved for future use" on the 28F016SA, is the V_{PP} Level bit on the 28F016SV. BSR.1 reflects the V_{PP} level applied to the 28F016SV (V_{PPH1} = "1," V_{PPH2} = "0"). See Table 2 for the 28F016SV's Block Status Register.

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Table 1. 28F016SV Compatible Status Register

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

CSR.7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy

CSR.6 = ERASE-SUSPEND STATUS
1 = Erase Suspended
0 = Erase In Progress/Completed

CSR.5 = ERASE STATUS
1 = Error In Block Erasure
0 = Successful Block Erase

CSR.4 = DATA-WRITE STATUS
1 = Error in Data Write
0 = Data Write Successful

CSR.3 = V_{PP} STATUS
1 = V_{PP} Error Detect, Operation Abort
0 = V_{PP} OK

CSR.2 - CSR.0 = RESERVED FOR FUTURE ENHANCEMENTS.
These bits are reserved for future use; mask them out when polling the CSR.

NOTES:

The RY/BY# output or WSMS bit must be checked to determine completion of an operation (erase suspend, erase or data write) before the appropriate Status bit (ESS, ES or DWS) is checked for success.

If DWS and ES are set to "1" during an erase attempt, an improper command sequence was entered. Clear the CSR and attempt the operation again.

The VPPS bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM periodically interrogates V_{PP}'s level only after the data-write or erase command sequences have been entered, and informs the system if it detects an invalid voltage. VPPS is not guaranteed to report accurate feedback between V_{PPLK}(max) and V_{PPH1}(min), between V_{PPH1}(max) and V_{PPH2}(min) and above V_{PPH2}(max).

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Table 2. 28F016SV Block Status Register

BS	BLS	BOS	BOAS	QS	VPPS	VPPL	R
7	6	5	4	3	2	1	0

BSR.7 = BLOCK STATUS
- 1 = Ready
- 0 = Busy

BSR.6 = BLOCK-LOCK STATUS
- 1 = Block Unlocked for Write/Erase
- 0 = Block Locked for Write/Erase

BSR.5 = BLOCK OPERATION STATUS
- 1 = Operation Unsuccessful
- 0 = Operation Successful or Currently Running

BSR.4 = BLOCK OPERATION ABORT STATUS
- 1 = Operation Aborted
- 0 = Operation Not Aborted

MATRIX 5/4
- 0 0 = Operation Successful or Currently Running
- 0 1 = Not a valid combination
- 1 0 = Operation Unsuccessful
- 1 1 = Operation Aborted

BSR.3 = QUEUE STATUS
- 1 = Queue Full
- 0 = Queue Available

BSR.2 = V_{PP} STATUS
- 1 = V_{PP} Error Detect, Operation Abort
- 0 = V_{PP} OK

BSR.1 = V_{PP} LEVEL
- 1 = V_{PP} detected at 5.0V ± 10% (4.5V - 5.5V)
- 0 = V_{PP} detected at 12.0V ± 5% (11.4V - 12.6V)

BSR.0 = RESERVED FOR FUTURE ENHANCEMENTS
This bit is reserved for future use; mask it out when polling the BSR.

NOTES:

The RY/BY# output or BS bit must be checked to determine completion of an operation (block lock, suspend, erase or data write) before the appropriate Status bits (BOS or BLS) is checked for success.

The BOAS bit will not be set until GSR.7 = 1.

Operation halted via abort command.

BSR.1 is not guaranteed to report accurate feedback between the V_{PPH1} and V_{PPH2} voltage ranges. Writes and erases with V_{PP} between V_{PPLK}(max) and V_{PPH1}(min), between V_{PPH1}(max) and V_{PPH2}(min), and above V_{PPH2}(max) produce spurious results and should not be attempted.
BSR.1 was a RESERVED bit on the 28F016SA.

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Table 3. 28F016SV Device Configuration Code

R	R	R	R	R	RB2	RB1	RB0
7	6	5	4	3	2	1	0

	NOTES:
DCC.2-DCC.0 = RY/BY# CONFIGURATION (RB2-RB0) 001 = Level Mode (Default) 010 = Pulse-On-Write 011 = Pulse-On-Erase 100 = RY/BY# Disabled 101 = RY/BY# Pulse-on-Write/Erase	Undocumented combinations of RB2-RB0 are reserved by Intel Corporation for future implementations and should not be used.
DCC.7-DCC.3 = RESERVED FOR FUTURE ENHANCEMENTS	These bits are reserved for future use; mask them out when reading the Device Configuration Code. Set these bits to 0 when writing the desired RY/BY# configuration to the device.

2.5 Device/Manufacturer IDs and Device Configuration Code

The 28F016SV shares the identical manufacturer and device identifiers as the 28F016SA, for full backwards-compatibility.

The 28F016SV retains the Device Revision Number of the 28F016SA, accessed via the Page Buffer after writing the Upload Device Information (99H) command sequence. The 28F016SV adds a Device Configuration Code, located at address 1EH in byte mode and address 0FH in word mode (lower 8 bits of 16-bit word), which allows system software to read the currently-configured 28F016SV RY/BY# mode. These data bits correspond to the bits written to the 28F016SV when configuring RY/BY# via the RY/BY Configuration (96H) command sequence. Unused bits of the Device Configuration Code are marked "reserved for future use" and should be masked out. See Table 3 for the 28F016SV's Device Configuration Code.

The 28F016SV also adds the Device Proliferation Code (01H), located at address 1FH in byte mode and address 0FH in word mode (upper 8 bits of 16-bit word). This code allows software identification of the 28F016SV versus the 28F016SA (described in Section 4.0).

2.6 Flowcharts

All 28F016SV and 28F016SA flowcharts are identical.

2.7 V_{PP} Voltage

The 28F016SV's V_{PP} Write/Erase voltage specifications offer the choice of either 5.0V ± 10% (4.5V–5.5V) or 12.0V ± 5% (11.4V–12.6V) operation during flash memory update. V_{PP} = 5.0V (V_{PPH1}) minimizes required chip count in designs where a suitable 12.0V supply is not already required for other system circuitry. V_{PP} = 12.0V (V_{PPH2}), on the other hand, provides significantly faster write and erase performance for applications that frequently alter flash memory contents, such as solid-state mass storage designs.

Tables 4–7 give write and erase specifications for the 28F016SV at V_{CC} = 3.3V/5.0V and at V_{PP} = 5.0V/12.0V. Performance numbers for erase and standard writes at 3.3V V_{CC}/12.0V V_{PP} (Table 5) and 5.0V V_{CC}/12.0V V_{PP} (Table 7) match those of the 28F016SA. Page Buffer writes are higher performance on the 28F016SV compared to the 28F016SA.

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Table 4. Write/Erase Performance (3,5)

V_{CC} = 3.3V ± 0.3V, V_{PP} = 5.0V ± 0.5V, T_A = 0° to +70°C

Parameter	Notes	Min	Typ(1)	Max	Unit	Test Conditions
Page Buffer Byte Write Time	2,6,7	TBD	8.0	TBD	µs	
Page Buffer Word Write Time	2,6,7	TBD	16.1	TBD	µs	
Byte Write Time	2,7	TBD	29.0	TBD	µs	
Word Write Time	2,7	TBD	35.0	TBD	µs	
Block Write Time	2,7	TBD	1.9	TBD	sec	Byte Write Mode
Block Write Time	2,7	TBD	1.2	TBD	sec	Word Write Mode
Block Erase Time	2,7	TBD	1.4	TBD	sec	
Full Chip Erase Time	2,7	TBD	44.8	TBD	sec	
Erase Suspend Latency Time to Read	4	1.0	12	75	µs	
Auto Erase Suspend Latency Time to Write		4.0	15	80	µs	

NOTES:

1. 25°C and nominal voltages.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Specification applies to interrupt latency for single block erase. Suspend latency for Erase All Unlocked Blocks Operation extends the maximum latency time to 270 µs.
5. Sampled, but not 100% tested. Guaranteed by design.
6. Assumes using the full Page Buffer to Wrtite to Flash (256 btes or 128 words).
7. The TBD information will be available in a technical paper. Please contact Intel's Application Hotline or your local sales office for more information.

Table 5. Write/Erase Performance (3,5)

V_{CC} = 3.3V ± 0.3V, V_{PP} = 12.0V ± 0.6V, T_A = 0° to +70°C

Parameter	Notes	Min	Typ(1)	Max	Unit	Test Conditions
Page Buffer Byte Write Time	2,6,7	TBD	2.2	TBD	µs	
Page Buffer Word Write Time	2,6,7	TBD	4.4	TBD	µs	
Word/Byte Write Time	2,7	5	9	TBD	µs	
Block Write Time	2,7	TBD	0.6	2.1	sec	Byte Write Mode
Block Write Time	2,7	TBD	0.3	1.0	sec	Word Write Mode
Block Erase Time	2	0.3	0.8	10	sec	
Full Chip Erase Time	2,7	TBD	25.6	TBD	sec	
Erase Suspend Latency Time to Read	4	1.0	9	55	µs	
Auto Erase Suspend Latency Time to Write		4.0	12	60	µs	

NOTES:

See Table 4 for Notes 1 through 7.

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Table 6. Write/Erase Performance (3,5)

V_{CC} = 5.0V ± 0.5V, 5.0V ± 0.25V, V_{PP} = 5.0V ± 0.5V, T_A = 0° to +70°C

Parameter	Notes	Min	Typ(1)	Max	Unit	Test Conditions
Page Buffer Byte Write Time	2,6,7	TBD	8.0	TBD	µs	
Page Buffer Word Write Time	2,6,7	TBD	16.0	TBD	µs	
Byte Write Time	2,7	TBD	20	TBD	µs	
Word Write Time	2,7	TBD	25	TBD	µs	
Block Write Time	2,7	TBD	1.4	TBD	sec	Byte Write Mode
Block Write Time	2,7	TBD	0.85	TBD	sec	Word Write Mode
Block Erase Time	2,7	TBD	1.0	TBD	sec	
Full Chip Erase Time	2,7	TBD	32.0	TBD	sec	
Erase Suspend Latency Time to Read	4	1.0	9	55	µs	
Auto Erase Suspend Latency Time to Write		3.0	12	60	µs	

NOTES:

See Table 4 for Notes 1 through 7.

Table 7. Write/Erase Performance (3,5)

V_{CC} = 5.0V ± 0.5V, 5.0V ± 0.25V, V_{PP} = 12.0V ± 0.6V, T_A = 0° to +70°C

Parameter	Notes	Min	Typ(1)	Max	Unit	Test Conditions
Page Buffer Byte Write Time	2,6,7	TBD	2.1	TBD	µs	
Page Buffer Word Write Time	2,6,7	TBD	4.1	TBD	µs	
Word Byte/Write Time	2,7	4.5	6	TBD	µs	
Block Write Time	2,7	TBD	0.4	2.1	sec	Byte Write Mode
Block Write Time	2,7	TBD	0.2	1.0	sec	Word Write Mode
Block Erase Time	2	0.3	0.6	10	sec	
Full Chip Erase Time	2,7	TBD	19.2	TBD	sec	
Erase Suspend Latency Time to Read	4	1.0	7	40	µs	
Auto Erase Suspend Latency Time to Write		3.0	10	45	µs	

NOTES:

See Table 4 for Notes 1 through 7.

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2.8 Other Voltage and Current Specifications

The 28F016SV's typical and maximum V_{CC} read and V_{CC} standby (CMOS levels) currents are both higher than those of the 28F016SA.

The 28F016SV's typical V_{CC} deep power-down current is higher than that of the 28F016SA. The 28F016SV will also exhibit higher V_{CC} current "peaks" in deep power-down mode at 3.3V V_{CC}, compared to the 28F016SA.

The 28F016SV adds the V_{PPH1} (V_{PP} = 5.0V) write/erase voltage specification and V_{CC} and V_{PP} write and erase current specifications at $V_{PP} = V_{PPH1}$. Write/erase current specifications at $V_{PP} = V_{PPH2}$ (12.0V) match those of the 28F016SA. The 28F016SV also lowers the V_{PPL} specification from 6.5V to 1.5V (to allow SmartVoltage operation) and renames this specification as V_{PPLK}, to signify the change. The 28F016SV's V_{CC}/V_{PP} erase suspend currents and V_{PP} read current ($V_{PP} > V_{CC}$) are lower than those of the 28F016SA.

Tables 8 and 9 show added and revised (as compared to the 28F016SA) 28F016SV DC specifications.

Table 8. 28F016SV Added/Revised DC Characteristics for 3.3V V_{CC} Operations

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
I_{CCS}	V_{CC} Standby Current		70	130	µA	$V_{CC} = V_{CC}$ Max CE_0#, CE_1#, RP# = V_{CC} ± 0.2V BYTE#, WP#, 3/5# = V_{CC} ± 0.2V or GND ± 0.2V
I_{CCD}	V_{CC} Deep Power-Down Current		2	5	µA	RP# = GND ± 0.2V BYTE# = V_{CC} ± 0.2V or GND ± 0.2V
$I_{CCR}1$	V_{CC} Read Current		40	50	mA	$V_{CC} = V_{CC}$ Max CMOS: CE_0#, CE_1# = GND ± 0.2V, BYTE# = GND ± 0.2V or V_{CC} ± 0.2V, Inputs = GND ± 0.2V or V_{CC} ± 0.2V TTL: CE_0#, CE_1# = V_{IL}, BYTE# = V_{IL} or V_{IH}, Inputs = V_{IL} or V_{IH} f = 8 MHz, I_{OUT} = 0 mA
$I_{CCR}2$	V_{CC} Read Current		20	30	mA	$V_{CC} = V_{CC}$ Max CMOS: CE_0#, CE_1# = GND ± 0.2V BYTE# = GND ± 0.2V or V_{CC} ± 0.2V, Inputs = GND ± 0.2V or V_{CC} ± 0.2V TTL: CE_0#, CE_1# = V_{IL}, BYTE# = V_{IL} or V_{IH}, Inputs = V_{IL} or V_{IH} f = 4 MHz, I_{OUT} = 0 mA

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Table 8. 28F016SV Added/Revised DC Characteristics for 3.3V V_{CC} Operations (Continued)
V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
I_{CCW}	V_{CC} Write Current		8	17	mA	V_{PP} = 5.0V ± 10% Word/Byte Write in Progress
I_{CCE}	V_{CC} Block Erase Current		9	17	mA	V_{PP} = 5.0V ± 10% Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current		1	4	mA	CE_0#, CE_1# = V_{IH} Block Erase Suspended
I_{PPR}	V_{PP} Read Current		30	200	µA	$V_{PP} > V_{CC}$
I_{PPW}	V_{PP} Write Current		15	25	mA	V_{PP} = 5.0V ± 10% Word/Byte Write in Progress
I_{PPE}	V_{PP} Erase Current		14	20	mA	V_{PP} = 5.0V ± 10% Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current		30	50	µA	$V_{PP} = V_{PPH1}$ or V_{PPH2} Block Erase Suspended
V_{PPLK}	V_{PP} Erase/Write Lock Voltage	0.0		1.5	V	
V_{PPH1}	V_{PP} during Write/Erase Operations	4.5	5.0	5.5	V	

Table 9. 28F016SV Added/Revised DC Characteristics for 5.0V V_{CC} Operations
V_{CC} = 5.0V ± 0.5V, 5.0V ± 0.25V, T_A = 0°C to +70°C

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
I_{CCS}	V_{CC} Standby Current		70	130	µA	$V_{CC} = V_{CC}$ Max CE_0#, CE_1#, RP# = V_{CC} ± 0.2V BYTE#, WP#, 3/5# = V_{CC} ± 0.2V or GND ± 0.2V
I_{CCD}	V_{CC} Deep Power-Down Current		2	5	µA	RP# = GND ± 0.2V BYTE# = V_{CC} ± 0.2V or GND ± 0.2V
I_{CCR}1	V_{CC} Read Current		75	95	mA	$V_{CC} = V_{CC}$ Max CMOS:CE_0#, CE_1# = GND ± 0.2V, BYTE# = GND ± 0.2V or V_{CC} ± 0.2V. Inputs = GND ± 0.2V or V_{CC} ± 0.2V TTL: CE_0#, CE_1# = V_{IL}, BYTE# = V_{IL} or V_{IH}, Inputs = V_{IL} or V_{IH} f = 10 MHz, I_{OUT} = 0 mA

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Table 9. 28F016SV Added/Revised DC Characteristics for 5.0V V_{CC} Operations (Continued)
V_{CC} = 5.0V ± 0.5V, 5.0V ± 0.25V, T_A = 0°C to +70°C

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$I_{CCR}2$	V_{CC} Read Current		45	55	mA	$V_{CC} = V_{CC}$ Max CMOS:CE_0#, CE_1# = GND ± 0.2V, BYTE# = GND ± 0.2V or V_{CC} ± 0.2V, Inputs = GND ± 0.2V or V_{CC} ± 0.2V TTL: CE_0#, CE_1# = V_{IL}, BYTE# = V_{IL} or V_{IH}, Inputs = V_{IL} or V_{IH} f = 5 MHz, I_{OUT} = 0 mA
I_{CCW}	V_{CC} Write Current		25	40	mA	V_{PP} = 5.0V ± 10% Word/Byte in Progress
I_{CCE}	V_{CC} Erase Suspend Current		20	30	mA	V_{PP} = 5.0V ± 10% Block Erase in Progress
I_{CCES}	V_{CC} Block Erase Current		2	4	mA	CE_0#, CE_1# = V_{IH} Block Erase Suspended
I_{PPR}	V_{PP} Read Current		30	200	µA	$V_{PP} > V_{CC}$
I_{PPW}	V_{PP} Write Current		17	22	mA	V_{PP} = 5.0V ± 10% Word/Byte Write in Progress
I_{PPE}	V_{PP} Block Erase Current		16	20	mA	V_{PP} = 5.0V ± 10% Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current		30	50	µA	$V_{PP} = V_{PPH1}$ or V_{PPH2} Block Erase Suspended
V_{PPLK}	V_{PP} Write/Erase Lock Voltage	0.0		1.5	V	

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2.9 Read Timing Specifications

The 28F016SV "bin 1"' significantly improves many read specifications compared to the 28F016SA. At 3.3V V_{CC}, read performance is almost 2x that of "bin 2." Tables 10 and 11 show these improved specifications.

Table 10. Improved 28F016SV AC Read Timing Characteristics for 3.3V V_{CC} Operations

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Version		28F016SV-075		Units
Symbol	**Parameter**	**Min**	**Max**	
t_{AVAV}	Read Cycle Time	75		ns
t_{AVQV}	Address to Output Delay		75	ns
t_{ELQV}	CE# to Output Delay		75	ns
t_{PHQV}	RP# High to Output Delay		480	ns
t_{GLQV}	OE# to Output Delay		40	ns
t_{EHQZ}	CE# to Output in High Z		30	ns
t_{FHQV}	BYTE# High to Output Delay		75	ns

Table 11. Improved 28F016SV AC Read Timing Characteristics for 5.0V V_{CC} Operations

V_{CC} = 5.0V ± 0.5V, 5.0V ± 0.25V, T_A = 0°C to +70°C

Versions		V_{CC} ± 5%	28F016SV-065			Units
		V_{CC} ± 10%		28F016SV-070		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	
t_{AVAV}	Read Cycle Time	65		70		ns
t_{AVQV}	Address to Output Delay		65		70	ns
t_{ELQV}	CE# to Output Delay		65		70	ns
t_{PHQV}	RP# High to Output Delay		300		300	ns
t_{GLQV}	OE# to Output Delay		30		35	ns
t_{FHQV}	BYTE# High to Output Delay		65		70	ns

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2.10 Write Timing Specifications

The 28F016SV write timing specifications have also been improved to keep read and write cycle times equivalent and to simplify system interface to the flash memory. Tables 12 through 15 show these improved specifications. Both WE#– and CE#–controlled write specifications are shown, for both commands and writes to the page buffer, and at V_{CC} = 3.3V and 5.0V.

Table 12. Improved 28F016SV AC WE#–Controlled Write Characteristics for 3.3V V_{CC} Operations
V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Version		28F016SV-075		Units
Symbol	**Parameter**	**Min**	**Max**	
t_{AVAV}	Write Cycle Time	75		ns
t_{ELWL}	CE# Setup to WE# Going Low	0		ns
t_{WLWH}	WE# Pulse Width	60		ns
t_{AVWH}	Address Setup to WE# Going High	60		ns
t_{DVWH}	Data Setup to WE# Going High	60		ns
t_{WHDX}	Data Hold from WE# High	5		ns
t_{WHAX}	Address Hold from WE# High	5		ns
t_{WHEH}	CE# Hold from WE# High	5		ns
t_{WHWL}	WE# Pulse Width High	15		ns
t_{PHWL}	RP# High Recovery to WE# Going Low	480		ns
t_{WHGL}	Write Recovery before Read	55		ns

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Table 13. Improved 28F016SV AC WE#–Controlled Write Specifications for 5.0V V_{CC} Operations

V_{CC} = 5.0V ± 0.5V, 5.0V ± 0.25V, T_A = 0°C to +70°C

Versions		V_{CC} ± 5%	28F016SV-065			Units
		V_{CC} ± 10%		28F016SV-070		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	
t_{AVAV}	Write Cycle Time	65		70		ns
t_{PHEL}	RP# Setup to CE# Going Low	300		300		ns
t_{AVWH}	Address Setup to WE# Going High	40		40		ns
t_{DVWH}	Data Setup to WE# Going High	40		40		ns
t_{WLWH}	WE# Pulse Width	40		45		ns
t_{WHAX}	Address Hold from WE# High	5		10		ns
t_{WHEH}	CE# Hold from WE# High	5		5		ns
t_{WHWL}	WE# Pulse Width High	15		15		ns
t_{PHWL}	RP# High Recovery to WE# Going Low	300		300		ns
t_{WHGL}	Write Recovery before Read	55		60		ns

Table 14. Improved 28F016SV AC CE#–Controlled Write Characteristics for 3.3V V_{CC} Operations

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Version		28F016SV-075		Units
Symbol	**Parameter**	**Min**	**Max**	
t_{AVAV}	Write Cycle Time	75		ns
t_{ELEH}	CE# Pulse Width	60		ns
t_{AVEH}	Address Setup to CE# Going High	60		ns
t_{DVEH}	Data Setup to CE# Going High	60		ns
t_{EHWH}	WE# Hold from CE# High	5		ns
t_{EHEL}	CE# Pulse Width High	15		ns
t_{PHEL}	RP# High Recovery to CE# Going Low	480		ns
t_{EHGL}	Write Recovery before Read	55		ns

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Table 15. Improved 28F016SV AC CE#–Controlled Write Characteristics for 5.0V V_{CC} Operations

V_{CC} = 5.0V ± 0.5V, 5.0V ± 0.25V, T_A = 0°C to +70°C

Versions		V_{CC} ± 5%	28F016SV-065			Units
		V_{CC} ± 10%			28F016SV-070	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	
t_{AVAV}	Write Cycle Time	65		70		ns
t_{PHWL}	RP# Setup to WE# Going Low	300		300		ns
t_{AVEH}	Address Setup to CE# Going High	40		45		ns
t_{DVEH}	Data Setup to CE# Going High	40		45		ns
t_{ELEH}	CE# Pulse Width	40		45		ns
t_{EHWH}	WE# Hold from CE# High	5		5		ns
t_{EHEL}	CE# Pulse Width High	15		15		ns
t_{PHEL}	RP# High Recovery to CE# Going Low	300		300		ns
t_{EHGL}	Write Recovery before Read	55		60		ns

3.0 HARDWARE DESIGN FOR FORWARDS-COMPATIBILITY

Manufacturers that wish to use the 28F016SA now, and move to the 28F016SV for write performance, integration or other reasons, should keep the following focus areas in mind when completing designs:

3.1 V_{CC} Voltage

As noted in Section 2.8, the 28F016SV's typical and maximum read/standby current and typical deep power-down current are higher than those of the 28F016SA. V_{CC} power supply selection should factor in these higher currents, as should system power consumption calculations. Decoupling and bypass capacitors can supply current for any of the 28F016SV V_{CC} deep power-down mode current "spikes" (V_{CC} = 3.3V) with no added burden on the power supply.

If conversion to the 28F016SV will also include changing the write/erase voltage to 5.0V from 12.0V, 5.0V power supply current calculations should include both the future additional write/erase current drawn by the 28F016SV's V_{CC} input (if V_{CC} = 5.0V) and the future current drawn by the 28F016SV's V_{PP} input (connected to 5.0V).

3.2 V_{PP} Voltage

Conversion to the 28F016SV may be driven by the desire to write/erase at 5.0V (thereby eliminating the need for a separate 12.0V regulator). Keep in mind that write/erase at 5.0V is lower performance than at 12.0V. Some flash memory applications (but not all) can tolerate this additional write/erase time. For these applications, a jumper on the system board that enables V_{PP} pin connection either to the output of a 12.0V converter (for the 28F016SA) or to the system 5.0V supply (for the 28F016SV) should be added. With the jumper connected to 5.0V, the 12.0V converter and associated circuitry can be removed to lower system component count. See Figure 3 for an example.

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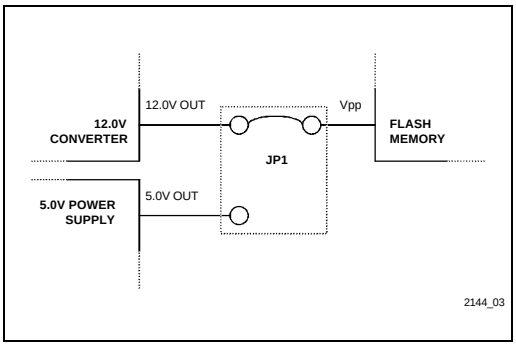

Figure 3. Jumper Selection of 12.0V Converter or 5.0V Power Supply Output for V_{PP}

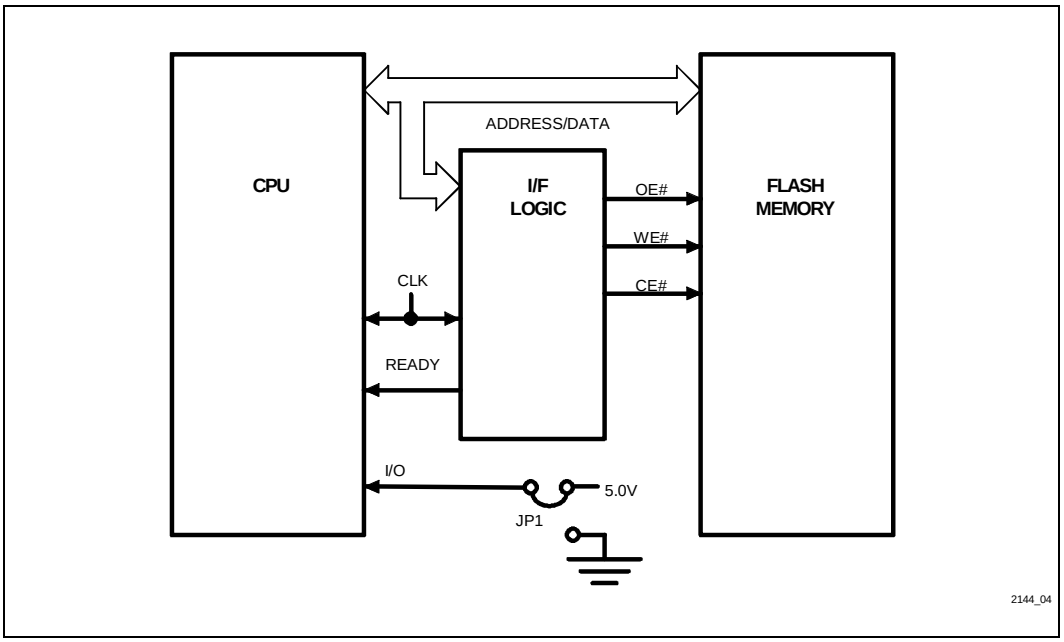

Figure 4. Jumper Identification of 28F016SA or 28F016SV Presence

Write Protection Via V_{PPLK}

Switching V_{PP} off during normal operation is one of several methods commonly used to prevent unwanted alteration (data write or erase) of flash memory data. Designs that use this technique should ensure that the V_{PP} voltage transitions to GND when "off." Some 12.0V converters drop V_{PP} to a diode drop below V_{CC} when they are placed in shutdown. This will block unwanted data write and erase on the 28F016SA but not on the 28F016SV, which has a 5.0V V_{PP} option. An external pulldown resistor will pull the converter output to GND, preventing data alteration on either the 28F016SA or the 28F016SV. Other write protection techniques (i.e., RP# and WP# control) should also be used for full flash memory data protection.

3.3 Read/Write Performance and Wait-State Configuration

Conversion to the 28F016SV may also be driven by its higher read performance. Component identification in communicating whether the 28F016SA or the high speed 28F016SV is in system can either be

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accomplished via hardware or software methods (see Sections 3.4 and 4.1). Depending which component resides in the system, the state machine within the interface logic and/or system software can modify the wait-state profile of the flash memory space to take advantage of the 28F016SV's higher read performance capability.

3.4 Hardware Identification of 28F016SA or 28F016SV

Jumpers can be used to communicate whether the 28F016SA or 28F016SV device is in the system, as shown in Figure 4. As the device identifiers for the 28F016SA and the 28F016SV are identical (see Section 4.1), software identification of one or the other flash memory via reading the device ID is not feasible. See Section 4.1 for a software method of identifying the 28F016SA or 28F016SV via the Device Proliferation Code. Jumper identification can also be used to enable system software usage of the 28F016SV's Status Register enhancements and Device Configuration Code. See Section 4 for more information

4.0 SOFTWARE DESIGN FOR FORWARDS-COMPATIBILITY

The 28F016SV is fully software backwards-compatible with the 28F016SA. This section discusses several 28F016SV enhancements that system software can access if desired. Keep in mind that these features are not available on the 28F016SA and their access and/or implementation should not be attempted when using the 28F016SA.

4.1 Software Identification of 28F016SA or 28F016SV

The 28F016SV's device identifier is identical to that for the 28F016SA. This enables all software written for the 28F016SA to be run on the 28F016SV unchanged. Methods of identifying the 28F016SV in the system, such as the jumper identification of Section 3.3 and Figure 3, can be used in designs that can accept both the 28F016SV and the 28F016SA. An alternative software method uses the Device Proliferation Code, supported on the 28F016SV (01H), but not on the 28F016SA. By initializing the Page Buffer location corresponding to this code to a known value and then executing an Upload Device Information command sequence, subsequent reads of the Page Buffer will identify the specific FlashFile memory in the system. The Device Proliferation Code address in the Page Buffer is 1FH in x8 mode and 0FH (upper 8 bits) in x16 mode. A pseudocode flow for this technique is shown below:

Initialize Device Proliferation Code address in Page Buffer to 00H.
Execute Upload Device Information command sequence
Swap Page Buffer
Read from Device Proliferation Code address
    If data = 00H, 28F016SA is present
    If data = 01H, 28F016SV is present
End

4.2 Block Status Register V_{PP} Level Bit

Bit 1 of the Block Status Registers, a "reserved" bit on the 28F016SA, is the "V_{PP} Level" bit on the 28F016SV (see Section 2.4 and Table 2). System software interfacing to the 28F016SV can examine this bit and, by determining what V_{PP} voltage is in the system, gain an indication of the level of Data Write and Erase performance to be expected. This capability is particularly valuable when creating software that could run either in a 12.0V V_{PP} or 5.0V V_{PP} system (such as a low-level PCMCIA driver). Knowledge of Write/Erase performance allows software to adjust the frequency and duration of events such as background media cleanup to optimize system performance.

4.3 Enhanced V_{PP} Status Bit

Bit 2 of the Block Status Registers, functionally identical to bit 3 of the Compatible Status Register, is enhanced on the 28F016SV to reflect both 5.0V and 12.0V V_{PP} capability (see Section 2.4 and Tables 1 and 2). With V_{PP} = V_{PPH2} at the beginning of Data Write/Erase, V_{PP} transitions above V_{PPH2}(max) or below V_{PPH2}(min) will, if detected, terminate Data Write/Erase and return error indication via CSR.3 = BSR.2 ="1" (this is 100% compatible with the 28F016SA function). With V_{PP} = V_{PPH1} at the beginning of Data Write/Erase, V_{PP} transitions above V_{PPH1}(max) or below V_{PPH2}(min) will, if detected, also terminate Data Write/Erase and return error indication via CSR.3 = BSR.2 = "1" (this is new to the 28F016SV). Accordingly, the CSR.3 = BSR.2 = "1" condition has been renamed from "V_{PP} Low" (the 28F016SA definition) to "V_{PP} Error."

4.4 RY/BY# Configuration

The 28F016SV adds the Device Configuration Code, accessible via the Page Buffer after first writing the Upload Device Information command sequence (see

Section 2.5 and Table 3). This code enables system software to read the currently-configured 28F016SV RY/BY# mode. The Device Configuration Code is located at Page Buffer address 1EH in x8 mode, 0FH (lower 8 bits in x16 mode).

As discussed earlier in Section 2.3, the 28F016SV includes an additional RY/BY# mode, RY/BY# Pulse on Write/Erase, enabled as part of the RY/BY# Configuration (96H) command sequence. This mode was "reserved for future use" on the 28F016SA.

5.0 CONCLUSION

This application note has summarized upgrade considerations and compatibility areas between the 28F016SA and the 28F016SV. Consult reference documentation for a more complete understanding of compatibility and device capabilities. Please contact your local Intel or distribution sales office for more information on Intel's flash memory products.

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6.0 ADDITIONAL INFORMATION

Order Number	Document/Tool
290528	28F016SV Datasheet
290489	28F016SA Datasheet
297372	16-Mbit Flash Product Family User's Manual
292092	AP-357 "Power Supply Solutions for Flash Memory"
292123	AP-374 "Flash Memory Write Protection Techniques"
292124	AP-375 "Upgrade Considerations from the 28F008SA to the 28F016SA"
292126	AP-377 "16-Mbit Flash Product Family Software Drivers, 28F016SA/28F016SV/28F016XS/28F016XD"
292127	AP-378 "System Optimization Using the Enhanced Features of the 28F016SA"
292163	AP-610 "Flash Memory In-System Code and Data Update Techniques"
292165	AB-62 "Compiling Optimized Code for Flash Memories"
297508	FLASHBuilder Utility
Contact Intel/Distribution Sales Office	28F016SV iBIS Models
Contact Intel/Distribution Sales Office	28F016SV VHDL Models
Contact Intel/Distribution Sales Office	28F016SV Timing Designer Library Files
Contact Intel/Distribution Sales Office	28F016SV Orcad and ViewLogic Schematic Symbols

7.0 REVISION HISTORY

Number	Description
-001	Original Version
-002	Added new RY/BY# mode of 28F016SV (Pulse-On-Write/Erase). Added/Revised DC/AC Characteristics based on 28F016SV Datasheet (Rev. 002) - Increased I_{CCR} Added to Tables 8 and 9. - Decreased I_{CCES}, I_{PPR}, I_{PPES} Added to Tables 8 and 9. - t_{PHOV} Added to Table 10. - t_{PHOV} and t_{GLOV} Added to Table 11. - t_{PHWL} Added to Table 12. - t_{PHEL}, t_{AVWH}, t_{DVWH}, t_{WLWH} and t_{PHWL} Added to Table 13. - t_{PHEL} Added to Table 14. - t_{PHWL}, t_{AVEH}, t_{DVEH}, t_{ELEH} and t_{PHEL} Added to Table 15. Tables 16 and 17 Consolidated into Tables 12 and 13. Added “Swap Page Buffer” to Pseudocode Example in Section 4.1.
-003	Added 3/5# pin to Figures 1 and 2; Updated Sections 1.0, 2.1 and 2.8 accordingly. Updated Tables 4–7 to reflect specifactions of latest datasheet revisions. Added “Erase Suspend Latency Time to Read” and “Auto Erase Suspend Latency Time to Write” Specifications to Tables 4–7. Increased I_{PPR} (V_{PP} Read Current) for $V_{PP} > V_{CC}$ to 200 µA at V_{CC} = 3.3V and V_{CC} = 5.0V Increased t_{PHQV} Specifications at 5.0V V_{CC} to 400 ns in Table 11. Updated Additional Information Section. Made minor cosmetic changes throughout document.

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