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APPLICATION NOTE

28F008SA Hardware Interfacing

BRIAN DIPERT
MCD MARKETING APPLICATIONS

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28F008SA HARDWARE INTERFACING

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1.0 INTRODUCTION

The 28F008SA FlashFile™ Memory is a very high performance 8 Mbit (8,388,608 bit) memory, organized as 1 Mbyte (1,048,576 bytes) of 8 bits each. The 28F008SA contains sixteen 64 Kbyte (65,536 byte) blocks, each block separately eraseable and capable of 100,000 byte write-block erase cycles. On-chip automation dramatically simplifies software algorithms, and frees the system microprocessor to service higher priority tasks during component data update. An enhanced system interface allows switching the 28F008SA into a deep powerdown mode during periods of inactivity, and gives a hardware indication of the status of the internal Write State Machine. High-speed access time allows minimal wait-state interfacing to microprocessor buses, and advanced packaging provides optimum density/in^2.

Features of the 28F008SA include:

- High-Density Symmetrically Blocked Architecture:
  - — Sixteen 64 Kbyte Blocks
- Extended Cycling Capability
  - — 100,000 Block Erase Cycles
  - — 1.6 Million Block Erase Cycles per Chip
- Automated Byte Write and Block Erase
  - — Command User Interface
  - — Status Register
- System Performance Enhancements
  - — RY/BY# Status Output
  - — Erase Suspend Capability
- Deep Powerdown Mode
  - — 0.20 μA I_{CC} Typical
- Very High Performance Read
  - — 85 ns Maximum Access Time
- SRAM-Compatible Write Interface
- Hardware Data Protection Features
  - — Erase/Write Lockout during Power Transitions
- Industry Standard Packaging
  - — 40 Lead TSOP, 44 Lead PSOP
- ETOX III Nonvolatile Flash Memory Technology
  - — 12V Byte Write/Block Erase

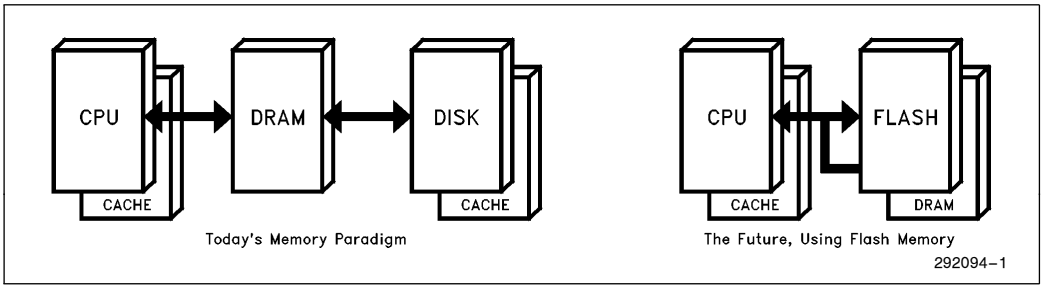


Figure 1. The 28F008SA Revolutionizes the Architecture of Computing

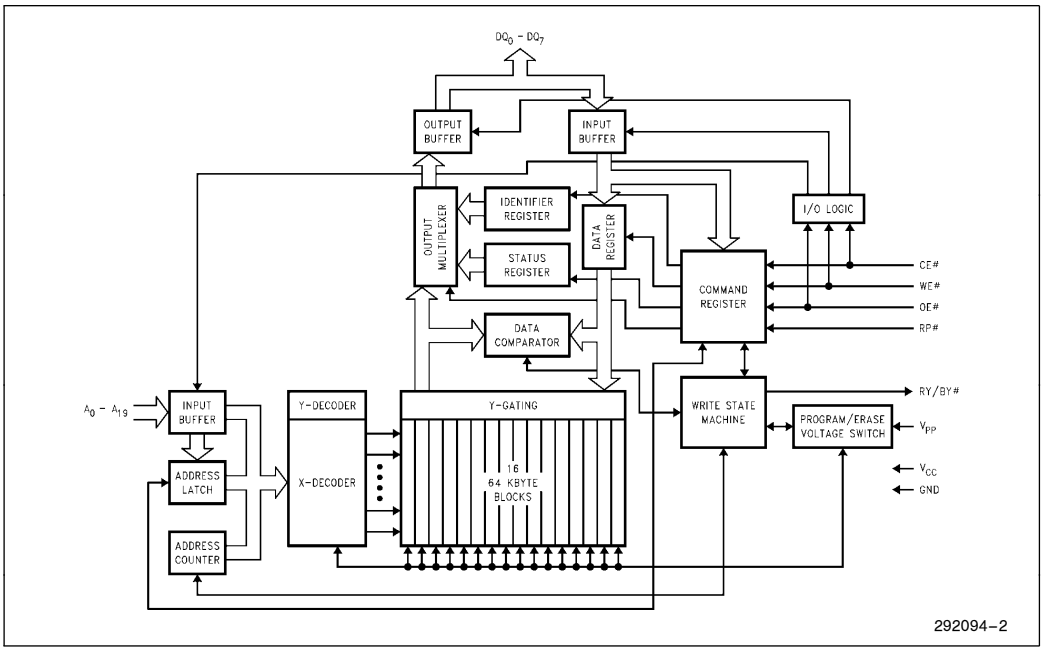


Figure 2. 28F008SA Block Diagram

Traditional system architectures combine slow, high density nonvolatile mass storage (such as a disk drive) and fast, volatile memory (such as DRAM) to fully address system requirements. As Figure 1 illustrates, flash memory combines the best features of both the above memory technologies, making a "disk/DRAM" approach to system architecture unnecessary and ultimately wasteful. Flash memory is rapidly approaching DRAM in both cost and performance (especially in cached systems), while adding capabilities (such as nonvolatility), that DRAM cannot claim. The 28F008SA will be the building block memory of choice for emerging computing markets, whether integrated in a memory card or disk drive form factor, or resident on the system motherboard.

This application note discusses hardware interfacing of the 28F008SA flash memory to system designs. The 28F008SA datasheet (order number 290429) is a valuable reference document, providing in-depth device technical specifications, package pinouts and timing waveforms. Additionally, companion application note AP-360, "28F008SA Software Drivers" (order number 292095) provides example ASM-86 and "C" routines for controlling the 28F008SA. AP-364 "28F008SA Automation and Algorithms" discusses in-depth operation of the 28F008SA Write State Machine and internal algorithms, emphasizing how they interface to system software and hardware. AP-360 and AP-364 should be reviewed in conjunction with this application note and the 28F008SA datasheet for a complete understanding of this device.

2.0 HARDWARE INTERFACING

Figure 2 shows a block diagram of the 28F008SA and its internal contents. The CE# (chip enable) and OE# (output enable) inputs have comparable enable and read functions to those of other memory technologies such as SRAM. Similarly, V_{CC} is the component power supply (5V ±10%), while GND should be connected to system ground. Address inputs allow the system to select a specific byte for reading or writing/erasing, and the 8-bit data bus transfers information to and from the 28F008SA. The other control lines (WE#, RP#, RY/BY# and V_{PP}) are discussed below.

2.1 V_{PP} (Byte Write/Block Erase Voltage)

The V_{PP} input supplies high voltage to the 28F008SA to enable byte write and block erase. V_{PP} is specified at 12V ±5% (11.4V–12.6V). Attempting to byte write or block erase the 28F008SA beyond the 5% 12V tolerance is not recommended. V_{PP} above 12.6V can potentially result in device damage, and V_{PP} below 11.4V dramatically lengthens write/erase time and compromises data reliability. The 28F008SA is guaranteed to prevent byte write and block erase attempts with V_{PP} below 6.5V, and in this situation it reports a "low V_{PP} error" through the component Status Register (see AP-360, AP-364 or the 28F008SA datasheet).

V_{PP} Generation Circuits

12V is often already present in systems, used to power the hard drive, display, RS-232 circuitry, flash BIOS update, etc. If it meets the tolerance and current capability requirements of the 28F008SA, such a power supply could be used directly as the 28F008SA update voltage source. However, 12V is sometimes not present or otherwise required, and in such cases, the 28F008SA V_{PP} must be derived from existing voltages and supplies.

Fortunately, flash memory's rapidly increasing popularity has driven ever-improving 12V converter availability in the market. These solutions derive a regulated 12V from a wide range of input voltages, and offer varied levels of integration and current delivery capability. In general, the input for 12V converters should come from the unregulated system power source, particularly in battery-powered systems.

Table 1 lists and briefly describes several 12V generation solutions available at the time this document was published. This is by no means an exhaustive list, and does not reflect any specific recommendation by Intel Corporation. For in-depth information on power supply solutions for flash memory, reference Intel application note AP-357 (order number 292092), available through your local Intel sales office or distributor.

Controlling V_{PP} to 28F008SA Component(s)

Once 12V is available in the system, how is it controlled? One approach is to hard-wire 12V from the supply directly to the V_{PP} inputs of each 28F008SA in the system. The advantage here is in design simplicity and board space savings. The 28F008SA Command User Interface architecture and two-step byte write/block erase command sequences provide protection from unwanted data alteration even with high voltage present on V_{PP}. All 28F008SA functions are disabled with V_{CC} below lockout voltage V_{LKO} (2.2V), or when RP# is at V_{IL} (see section 2.3). This provides data protection during system powerup, when the minimally-loaded V_{PP} supply often ramps to 12V before V_{CC} (and therefore control inputs to the device) are stable.

For additional data protection, the system designer can choose to make the V_{PP} supply switchable via a GPIO (General Purpose Input/Output) line, enabling 12V to the 28F008SA only during byte write or block erase attempts. A switchable V_{PP} also minimizes power consumption by both the flash memory components and the 12V supply or converter (due to efficiency losses). Many 12V converters integrate an ENABLE input, eliminating external circuitry. If such an input is not available, a low drain-source resistance MOSFET switch such as the Motorola MTD4P05 can be used at the 12V supply output. An example schematic for this switch is shown in Figure 3. The calculations below show that the low drain-source resistance of the MTD4P05 will keep a 12V input within the 5% tolerance required by the 28F008SA.

$R_{DS} = 0.6\Omega$

$I_{PP} = 60$ mA

(worst case, two components being byte written or block erased)

ΔV_{SWITCH} DROP $= (60\text{ mA} \times 0.6\Omega) = 0.04V$

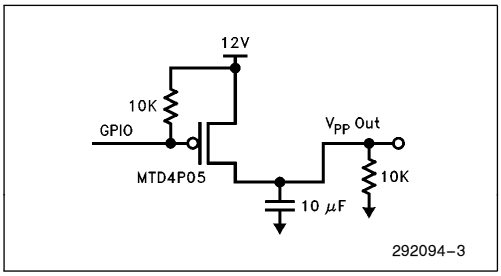


Figure 3. V_{PP} Switch Schematic

Table 1. 12V Conversion Solutions for V_{PP}

Manufacturer	Part Number	Input (V)	Package	Current Output	Total Components Needed	Est. Cost (10K)
Maxim	MAX732	4 to 7.5	16 SOIC	120 mA	9	$3.93
Linear Technology	LT1110-12	4.5 to 5.5	SO8	120 mA	11	$4.58
Linear Technology	LT1109-12	4.5 to 5.5	SO8	60 mA	8	$3.61
Motorola	MC34063A	4.5 to 5.5	SO8	120 mA	15	$2.25
Maxim	MAX667	12.1 to 16.5	SO8	120 mA	4	$2.63
Linear Technology	LT1111-12	16 to 30	SO8	120 mA	7	$3.95
National Semiconductor	LM2940CT-12	13 to 26	TO-220	1A	3	$1.30

2.2 RY/BY# (Ready/Busy) Output

The 28F008SA offers similar automated byte write/block erase capabilities to those first seen in the 28F001BX Bootblock flash memory family, introduced by Intel in May of 1991. It enhances these capabilities via the RY/BY# output, which provides hardware indication of internal Write State Machine (WSM) operation. RY/BY# is a full CMOS output, constantly driven by the 28F008SA and not tristated if the device CE# or OE# inputs are brought to V_{IH}. RY/BY#'s default state after device powerup is V_{OH}. It transitions low to V_{OL} when a byte write or block erase sequence is initiated by system software, and RY/BY#'s rising edge (return to V_{OH}) alerts the system to byte write or block erase completion. RY/BY# also goes to V_{OH} after the 28F008SA is put in Erase Suspend or Deep Powerdown modes.

RY/BY# is intended to interface the 28F008SA to a system microprocessor rising-edge-triggered interrupt input. In a multiple-chip memory array, external EPLD logic or an interrupt controller can be used to combine and prioritize RY/BY#s into one system interrupt (see Figure 4). The system can then, using a flash memory "activity table" set up in RAM, poll the individual 28F008SA Status Registers to determine which device has returned "ready", or read the RY/BY# inputs directly at the EPLD, as shown.

Figure 5 provides an alternative method for connecting multiple RY/BY#s to one interrupt input. The diode/resistor combination converts the 28F008SA full CMOS output into an open-drain "wired-OR" equivalent. Any RY/BY# at V_{OL} will drive the interrupt input low, and this input is pulled high by the resistors when all RY/BY#s are at V_{OH}. It is important in a design like this to use diodes with low forward voltage drops, so that the 28F008SA V_{OL} (0.45V) plus the diode voltage drop is still less than or equal to the destination input V_{IH} (0.8V). For the schematic shown in Figure 5, the equation is:

$$V_{OL} + V_{DIODE} = 0.45\ V_{MAX} + 0.3V = 0.75V \leq 0.8V$$

Note that should the system connect RY/BY# to an interrupt, disable that interrupt prior to suspending erase, as RY/BY# will transition to V_{OH} when the device is suspended.

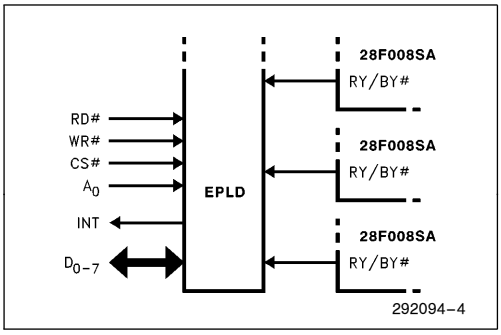


Figure 4. EPLD-Based RY/BY# Implementation

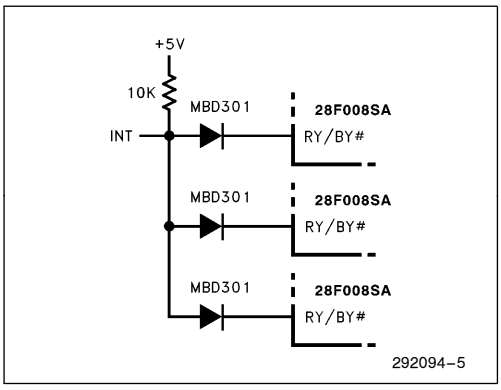


Figure 5. "Wired-OR" RY/BY# Implementation

2.3 RP# (Reset/Powerdown) Input

Deep Powerdown Mode

The RP# input, when driven to V_{IL} by the system, switches the 28F008SA into a deep powerdown mode with negligable power consumption. This feature integrates the V_{CC} power FET often used with low power designs. Power consumption thru V_{CC} is typically 1 μW in deep powerdown mode. RP#-low deselects the memory, places output drivers for D_{0-7} in a high-impedence state and turns off a majority of internal circuits. RY/BY# is driven to V_{OH} while in deep powerdown mode. Depending on the flexibility desired, system designers can choose to put either the entire flash device array into deep powerdown mode, or any individual components via selective input control. The 28F008SA requires a "wakeup" time after RP# returns to V_{IH} before it can be successfully written (t_{PHWL}) or outputs are valid to read attempts (t_{PHQV}).

Write Protection

Since RP# = V_{IL} deselects the 28F008SA, this input can be used not only as a means of entering deep powerdown mode but also as an active-high "chip enable" to block spurious writes during system power transitions. Figure 6 shows one possible RP# implementation, controlled by a GPIO line for power management and by a system POWER GOOD for power sequencing protection. In this design, the 5V monitoring circuit begins functioning at V_{CC} = 1V, and will enable the device only after V_{CC} transitions above 4.6V (and system control signals are therefore stable). As V_{CC} drops below 4.6V during system powerdown, RP# protection is again activated.

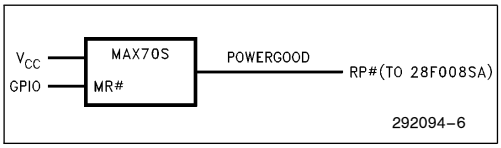


Figure 6. RP# Gating

Reset Control

RP# at V_{IL} resets all internal automation within the 28F008SA as part of the deep powerdown process. Upon exit from deep powerdown, the 28F008SA is reset to Read Array mode. This functionality is ideal when the 28F008SA is the boot memory for the system. RP# active transitions reset the Write Status Machine if system reset occurs during flash memory program or erase, and allow successful CPU reboot.

2.4 WE# (Write Enable) Input

When flash memory is written, the result can range from a 28F008SA that is placed in "read intelligent identifier" or "read Status Register" modes to alteration of nonvolatile flash memory contents. System hardware can prevent spurious writes to flash memory by application software or an operating system by gating the system WE# to flash memory components to enable writes only when desired.

Figure 7 shows a simple design that gates WE# with a GPIO line, enabling writes to the 28F008SA only when the GPIO is a "0". The GPIO is initialized to "1" on system powerup and the BIOS, a dedicated update software routine, a special keyboard sequence, switch on the back of the system or jumper on the system motherboard can then control the GPIO. This circuit ensures that flash memory contents are as permanent as "ROM" unless alteration is specifically desired.

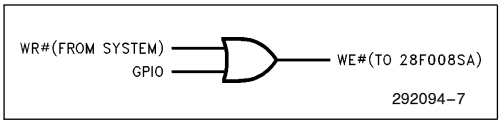


Figure 7. WE# Gating

2.5 High Density/In^2 Layout

Figure 8 shows an 8 Mbyte flash memory array using TSOP (Thin Small Outline)-packaged 28F008SAs in standard (E) and reverse (F) configurations. A layout like this is used in Intel's Series 2 flash memory cards (in densities to 20 Mbytes) and provides optimum array density for available board space.

Address and data lines are connected to all components in parallel. OE# and WE# are similarly connected. Section 2.7 of this document discusses alternate methods of implementing these signals for highest speed reads and writes in large memory arrays.

Component RY/BY#s are shown as not connected in Figure 8. They can be left unused, in which case the system software will substitute polling of component Status Registers for hardware interrupt, or RY/BY#s can be implemented as described in section 2.2.

CE#s are also not connected, intended to be individually driven by system chip enable decoding logic. This provides capability to read from and write to the array on a byte-by-byte basis. In a x16-only system, upper and lower byte 28F008SAs can have their CE#s bused together if desired.

Finally, V_{CC}, V_{PP} and RP# are connected in parallel to all components. Section 2.6 discusses bypass capacitor filtering of supply voltage inputs, while section 2.3 provides uses for RP#. If desired, individual component, component pair, etc. selective powerdown control can be substituted for the global control shown in Figure 8.

In space-constrained designs, a multiple-layer partial "serpentine" trace layout at the edges of the 28F008SA array may be implemented, with a full serpentine layout within the array as in Figure 8.

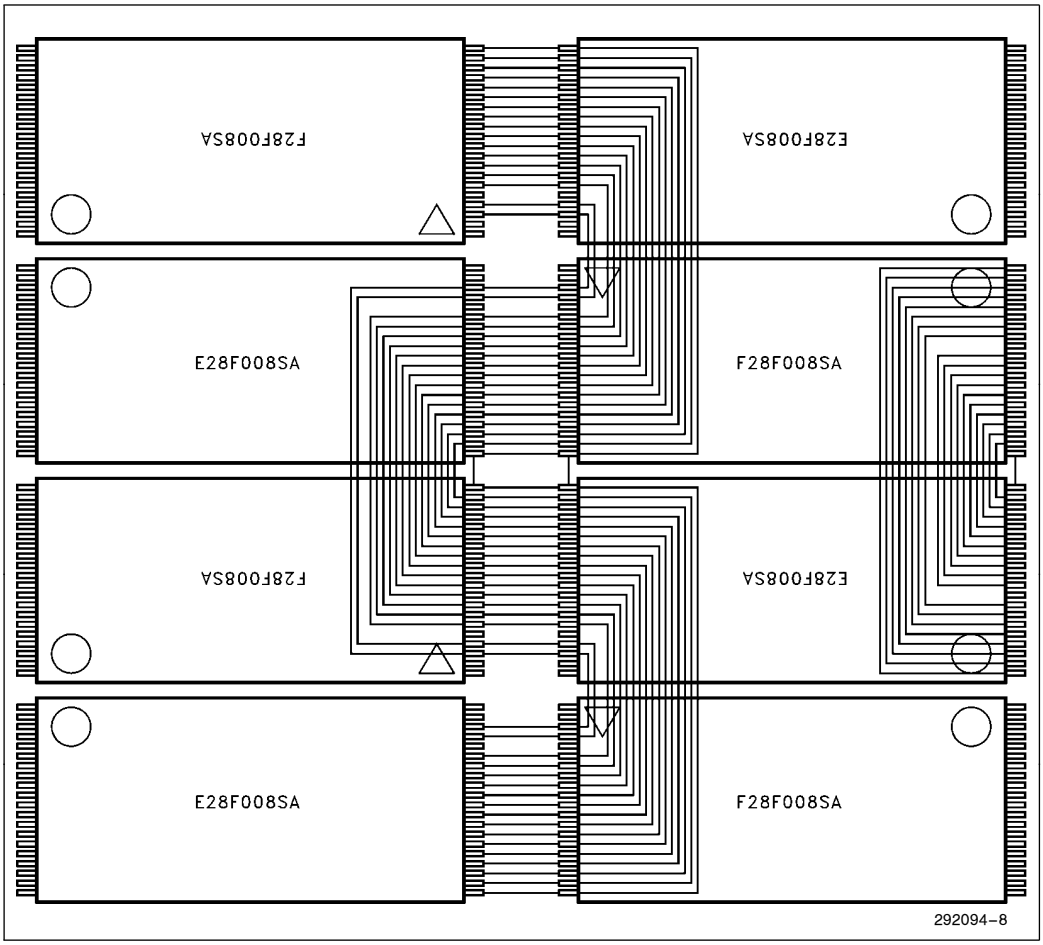


Figure 8. TSOP Serpentine Layout

2.6 Power Supply Decoupling

Both the V_{CC} and V_{PP} inputs to each 28F008SA should be decoupled at the package leads to provide noise immunity and supply current for transient current spikes during read, byte write and block erase. Additional bulk capacitance for groups of flash memories overcomes voltage slump caused by PC board trace inductances. Calculations for individual component and bulk capacitors (one per 8 devices) are shown below.

Basic Equation:

$I = C\ dv/dt$

Assumptions:

$I = 35$ mA per device (V_{CC}), therefore
$I = 17.5$ mA per device input (V_{CC})
$I = 30$ mA per device (V_{PP})
$dv = 0.1V$ (0.2V peak-peak)
$dt = 20$ ns

Per-Component-Input Decoupling Capacitor (V_{CC}):

$$C = I\ dt/dv = (17.5\ mA \times 20\ ns)/0.1V = 3.5\ nF$$

$$4x\ margin = 4 \times 3.5\ nF = 14\ nF$$

Standard Equivalent = **0.01 μF**

NOTE:
Calculations above assume that each 28F008SA is driving CMOS inputs (with corresponding high impedance and negligible input current requirements). If 28F008SA outputs are driving non-CMOS inputs, larger per-component capacitance may be needed to supply current while outputs are switching.

Bulk Capacitor (V_{CC}):

$$C = 10 \times \text{(Total of Decoupling Capacitors)}$$

$$\text{Bulk Capacitor (4 Mbyte array)} = 10 \times (8 \times 0.01\ \mu F) = 0.8\ \mu F$$

$$\text{Standard Equivalent} = \mathbf{1\ \mu F}$$

Per-Component Decoupling Capacitor (V_{PP}):

$$C = I\ dt/dv = (30\ mA \times 20\ ns)/0.1V = 6\ nF$$

$$\text{4x margin} = 4 \times 6\ nF = 24\ nF$$

$$\text{Standard Equivalent} = \mathbf{0.033\ \mu F}$$

2.7 High Speed Design Techniques

The 28F008SA's fast read access and command write specifications make it a natural choice for high performance memory arrays. The following tips will optimize the memory interface for optimum read/write speed. The common recommendation in all instances centers around minimizing fanout and capacitive bus loading to allow highest switching speed, lowest rise and fall times, and therefore greatest performance.

- Minimize address bus loading from the microprocessor to the memory array. Multiple address latches feeding subsets of the array speed address input to each 28F008SA and CE# decoding by external logic.
- Similarly, drive the memory array with multiple OE#s and WE#s. Most EPLD and discrete logic timing is specified at a 30 pF load, which equates to driving 4 28F008SA inputs at maximum input capacitance. Anything more than this may severely impact the logic's propagation delay.
- Finally, remember that each 28F008SA, when read, drives not only the system microprocessor or transceiver but also any other flash memory components connected to the common data bus. Each 28F008SA data output is specified at 12 pF, and the 28F008SA read timings are tested at either 30 pF or 100 pF of loading, depending on the chosen speed bin.

For large flash arrays where sequential data can be distributed on many devices, hardware interleaving provides additional performance.

2.8 Example Bus Interfaces

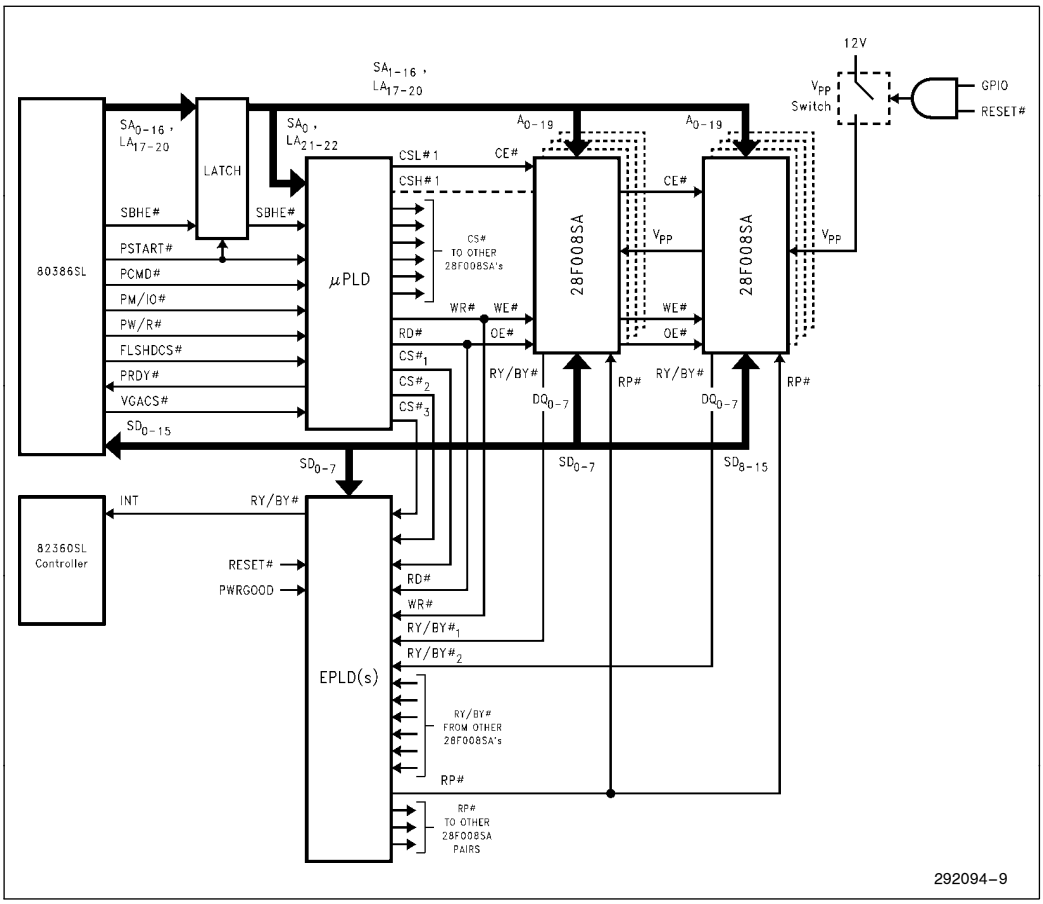
Appendix A shows hardware interface to the Intel386™SL PI bus, and Appendix B shows interface to the Intel486™SX local CPU bus. Both interfaces incorporate techniques described in sections 2.1–2.7 of this document. These designs are intended to be examples which can be modified to suit requirements of the end system.

ADDITIONAL INFORMATION

		Order Number
	28F008SA Datasheet	290429
	28F008SA-L Datasheet	290435
AP-357	"Power Supply Solutions for Flash Memory"	292092
AP-360	"28F008SA Software Drivers"	292095
AP-364	"28F008SA Automation and Algorithms"	292099
ER-27	"The Intel 28F008SA Flash Memory"	294011
ER-28	"ETOX-III Flash Memory Technology"	294012

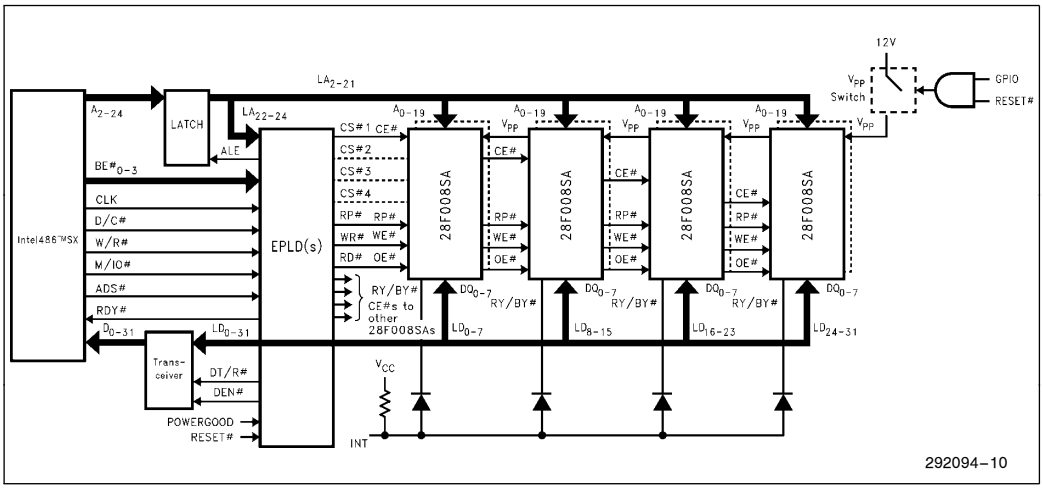
APPENDIX A

Intel386™SL PI BUS INTERFACE



NOTE:
The DRAM interface is not shown, for graphic simplicity.

APPENDIX B
Intel486™ SX LOCAL CPU BUS INTERFACE



NOTE:
The DRAM interface is not shown, for graphic simplicity.

REVISION HISTORY

Number	Description
-003	Renamed PWD# as RP# to match JEDEC conventions. Updated Figure 6 Added Reset Control discussion for RP# (Reset/Powerdown) Input.