SERIES 100
FLASH MEMORY
MINIATURE CARD
SPECIFICATION UPDATE

Release Date: February 1997

Order Number 297717-003

The iFM002A and iFM004A may contain design defects or errors known as errata. Characterized errata that may cause the iFM002A and iFM004A's (Series 100 Miniature Cards) behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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Germany 44-0-1793-421-333 other Countries 708-296-9333

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REVISION HISTORY

Date of Revision	Version	Description
09/01/96	-001	Original All updates were included in revision -002 of the *Series 100 Flash Memory Miniature Card Datasheet*, order number 290581-002
12/02/96	-002	Adds functional errata
02/01/97	-003	Corrects which errata applies to which steppings

PREFACE

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This is the third release of the Series 100 Miniature Card Specification Update. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published.

Functional descriptions for this product are found in the *Series 100 Flash Memory Miniature Card Datasheet*.

Affected Documents/Related Documents

Title	Order
Series 100 Flash Memory Miniature Card	290581-002

Nomenclature

Errata are design defects or errors. These may cause the Miniature Card's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation.

Documentation Changes include typos, errors, or omissions from the current published specifications.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLES OF CHANGES

The following tables indicate the Errata, Specification Changes, Specification Clarifications, or Documentation Changes which apply to *Series 100 Flash Memory Miniature Card*. Intel may fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▏	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Number	Steppings	Page	Status	Errata
1	A, B, C, D	7	Fix	CE# Deassertions When V_{CC} = 3.3V
2	E, F	8	Fix	CE# Deassertions When V_{CC} = 3.3V
3	A, B, C, D	9	Fix	CE# Glitch Sensitivity
4	A, B, C, D, E, F, G	11	Fix	Block Locking

Specification Changes

Number	Steppings	Page	Status	Specification Changes
1	A, B, C	12	Fix	AIS Corrections

Specification Clarifications

Number	Steppings	Page	Status	Specification Clarifications
N/A		13		None in this Specification Update revision.

Documentation Changes

Number	Steppings	Page	Status	Documentation Clarifications
N/A		13		None in this Specification Update revision.

IDENTIFICATION INFORMATION

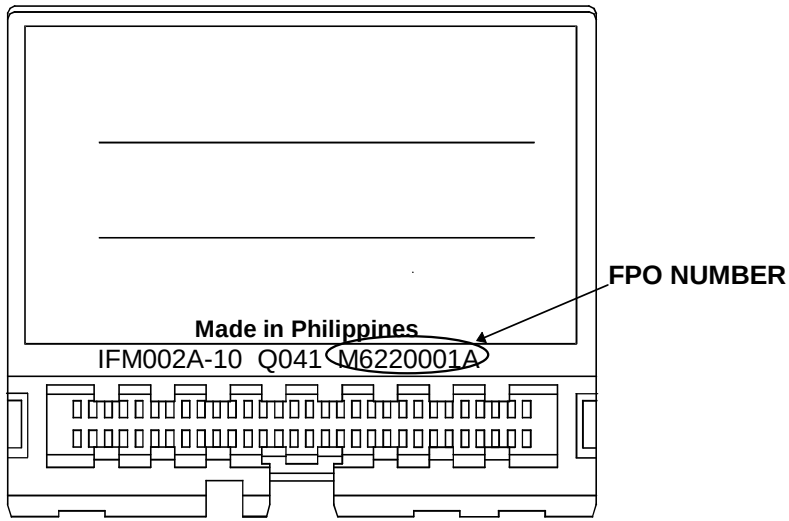
Markings

The Finished Processing Order (FPO) number correlates to a specific device stepping as illustrated in the table below:

Stepping(1)	Identifier
A through H Stepping	Last digit of the FPO number is A through H respectively.

NOTE:

1. Device steppings are based on continuous updates made in manufacturing and testing of the device and represent the current material shipped.



An FPO number contains the following information that describes the origin of the card:

The first character denotes the assembly site where "M" = Manila. The next character is the last digit of the year in which the unit was manufactured. In the above example, the unit was built in 1996. The next two digits are the week in the year. The remaining four digits are the lot number, and the last letter is the stepping. The above example shows a unit that was from lot 0001, built in Manila during week 22 of 1996. The last digit denotes that it is an A-step unit.

ERRATA

1. CE# Deassertions When V_{CC} = 3.3V

PROBLEM: The Miniature Card can return incorrect data if more than 15 successive read operations are performed where the CE# inputs are deasserted for more than 50 ns and less than 40 µs between each operation, and fewer than three locations are read during the operation. When the data is incorrect, bits that should be ones are read as zeros.

IMPLICATION: Systems that apply a series of short CE# deassertions are in jeopardy of reading incorrect data. This applies only to cards operating with V_{CC} = 3.3V.

WORKAROUND: There are two ways to prevent this problem:

1. Read more than two different locations for each assertion of CE#. This would typically be the case if the CPU were executing directly from the Miniature Card, because that involves primarily back-to-back reads from nearly sequential locations. In this case, the CE#s are deasserted for very brief periods of time (<50 ns) if at all.
2. Deassert CE# for more than 40 µs between all or most of the reads.

If it is suspected that an offending series of read operations has been performed, there are several ways of returning the Miniature Card to correct operation.

1. Program one location, even if the data written is FFFFh. This program command will not change any of the contents of the memory array contents, but in the course of getting ready to program a location, the memory devices will correct the problem.
2. Put the card in standby mode, deassert the appropriate CE#, for more than 1 ms.
3. Assert CEL# or CEH#, drive them low, for at least 330 µs.

These recovery methods are not destructive, so they can be performed as often as necessary to ensure that correct data will be read.

STATUS: This erratum will be fixed in future steppings.

AFFECTED PRODUCTS: This erratum applies to the A through D steppings of the Series 100 Miniature Cards.

2. CE# Deassertions When V_{CC} = 3.3V

PROBLEM: The Miniature Card can return incorrect data if more than 15 successive read operations are performed where the CE# inputs are deasserted for more than 100 ns and less than 500 ns between each operation, and fewer than three locations are read during the operation. When the data is incorrect, bits that should be ones are read as zeros.

IMPLICATION: Systems that apply a series of short CE# deassertions are in jeopardy of reading incorrect data. This applies only to cards operating with V_{CC} = 3.3V.

WORKAROUND: There are a two ways to prevent this problem:

1. Read more than two different locations for each assertion of CE#. This would typically be the case if the CPU were executing directly from the Miniature Card, because that involves primarily back-to-back reads from nearly sequential locations. In this case, the CE#s are deasserted for very brief periods of time (<50 ns) if at all.
2. Deassert CE# for more than 500 ns between all or most of the reads.

If it is suspected that an offending series of read operations has been performed, there are several ways of returning the Miniature Card to correct operation.

1. Program one location, even if the data written is FFFFh. This program command will not change any of the contents of the memory array contents, but in the course of getting ready to program a location, the memory devices will correct the problem.
2. Put the card in standby mode, deassert the appropriate CE#, for more than 1 ms.
3. Assert CEL# or CEH#, drive them low, for at least 330 µs.

These recovery methods are not destructive, so they can be performed as often as necessary to ensure that correct data will be read.

STATUS: This erratum will be fixed in future steppings.

AFFECTED PRODUCTS: This erratum applies to the E and F steppings of the Series 100 Miniature Cards.

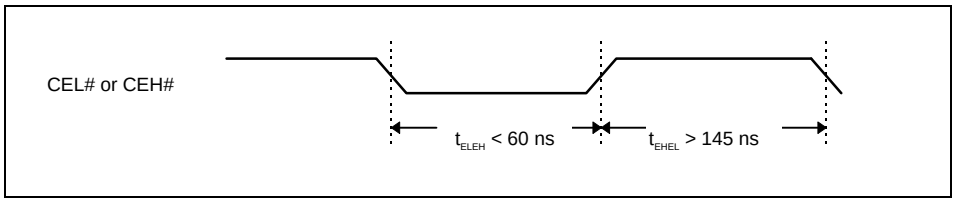
3. CE# Glitch Sensitivity

PROBLEM: If certain sequences of control signals are repetitiously applied, and if a read operation is performed immediately after, then that read operation could return data in which bits that should be zeros are returned as ones.

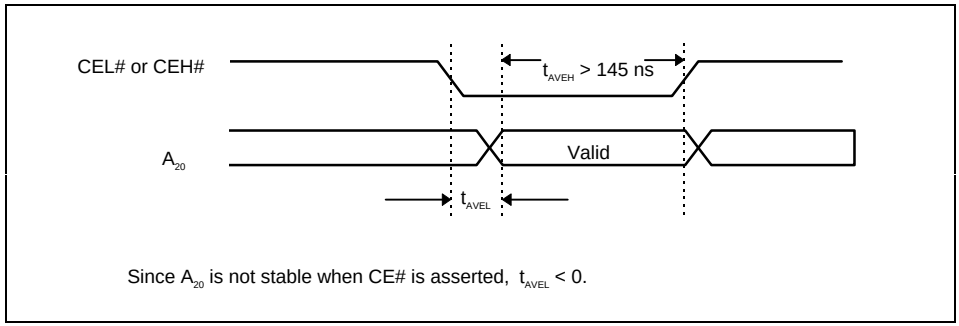
There are two sequences of control signals that have been observed to cause the errant reads.

1. Either or both CE# inputs is asserted for less than 60 ns. This is depicted in *CE# Glitch* illustration, below.
2. On a 4-Mbyte card, the A_{20} input is not stable prior to the assertion of either or both CE# inputs (the A_{20} input is not connected on the 2-Mbyte card). Refer to Figure A_{20} *Lags CE#*, below.

If either of these sequences of control inputs are repetitiously applied, incorrect data can be returned in subsequent reads.



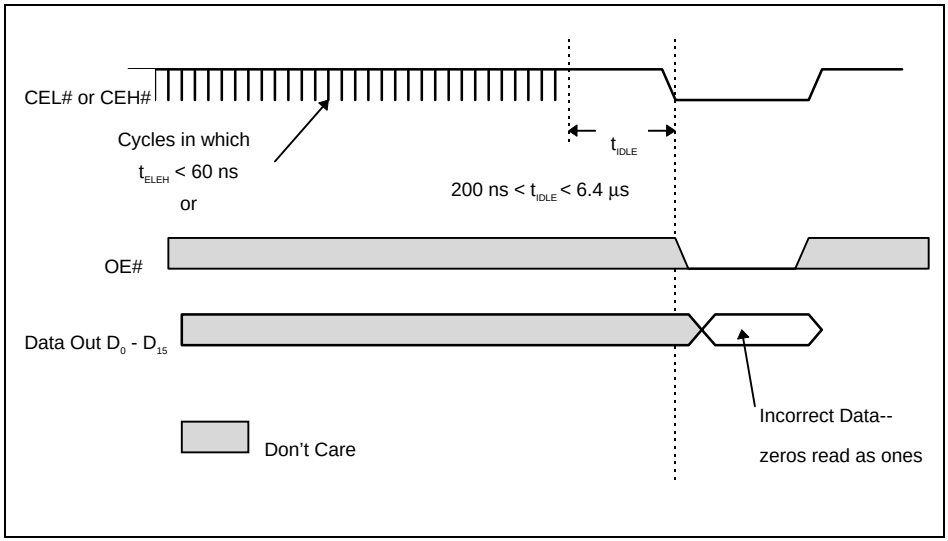
CE# Glitch



A_{20} Lags CE#

A single application of the above sequences does not cause an errant read. The problem has only been observed after several hundred of either of the above sequences, and even then it is very intermittent.

The most likely operation that could cause this condition is erasing one set of chip-pairs in a 4-Mbyte card, and polling the chips continuously until they are finished. While the chip pair is erasing, hundreds or thousands of read operations are performed on that chip pair. If the card controller hardware applies a glitch to the other chip pair—the pair that is not being erased—an incorrect read could result when the other chip pair is read. Refer to *A Series of CE# Glitches* for an illustration of this problem.



A Series of CE# Glitches

IMPLICATION: Once an offending series of glitches has been applied, data read from the card is suspect. This is a read issue only. There are no issues with programming or erasing.

It is straightforward to determine if a system is sensitive to this erratum. On a 2-Mbyte card, look for glitches on the CE# inputs. On a 4-Mbyte card, observe the CE#s and A_{20}. If they exhibit the timing shown, then the system could experience this problem.

Finally, this problem was observed very infrequently on a few systems when using 4-Mbyte cards. In those systems, the controller applied A_{20} about 30 ns after CE# was asserted. This caused one chip-pair to experience a glitch just prior to the second chip-pair being read.

WORKAROUND: If it is suspected that the Miniature Card socket controller is causing glitches, there are three ways that the card can be returned to the state where it is reliably reading data.

1. Perform a single word write operation, even one where the data written is all ones. A word write operation consists of a setup command—40h to recover from CEL#, 4000h for CEH# or 4040 for CEL# and CEH—followed by the data. If the data written is all ones, then the contents of the card will not be changed. Any zeros written to the array will be written correctly.
2. Put the card in standby mode, deassert CE#, for more than 50 ms.
3. Assert CEL# or CEH#, drive them low, for at least 13 µs.

STATUS: This erratum will be fixed in future steppings.

AFFECTED PRODUCTS: This erratum applies to the A through D steppings of the Series 100 Miniature Cards.

4. Block Locking

PROBLEM: Block Locking is not functional.

IMPLICATION: Program and erase are 100% functional, but individual blocks cannot be locked. A program or erase command issued to a location or block will always be executed; therefore, do not assume that any block cannot be modified.

WORKAROUND: Use the Write-protect switch to protect a card if there is data on the card that must be protected.

STATUS: This erratum will be fixed in future steppings

AFFECTED PRODUCTS: This erratum applies to A through G steppings of the Series 100 Miniature Cards.

SPECIFICATION CHANGES

1. AIS Corrections

DESCRIPTION: Some of the information in the AIS is incorrect. The following tables list the affected locations, the current contents and what the contents should be.

2-Mbyte Card

Location	Description	Current Contents	New Contents
43H	2 Mbyte	02H	01H
45H	150 ns (3.3V Access Time)	15H	0FH
46H	100 ns (5.0V Access Time)	10H	0AH

4-Mbyte Card

Location	Description	Current Contents	New Contents
43H	4 Mbyte	04H	03H
45H	150 ns (3.3V Access Time)	15H	0FH
46H	100 ns (5.0V Access Time)	10H	0AH

AFFECTED PRODUCTS: These changes to the AIS will be made to Miniature Cards built after week 47 of 1996.

SPECIFICATION CLARIFICATIONS

There are no specification clarifications in this Specification Update revision.

DOCUMENTATION CHANGES

There are no documentation changes in this Specification Update revision.