ADVANCE INFORMATION

SERIES 100 FLASH MEMORY MINIATURE CARD

iFM002A, iFM004A

- **Low-Cost Linear Flash Card**
- **Miniature Card Specification Compliant**
- **Single Supply SmartVoltage Operation**
  - **5V or 3.3V Read/Write**
- **Fast Read Performance**
  - **100 ns Max Access Time at 5V**
  - **150 ns Max Access Time at 3.3V**
- **x16 Data Interface**
- **High-Performance Random Writes**
  - **8 µs Typical Word Write at 5V**
  - **17 µs Typical Word Write at 3.3V**
- **100 µA Maximum Deep Power-Down**
- **Automated Write and Erase Algorithms**
  - **28F008SC Command Set**
- **Enhanced Automated Suspend Options**
  - **Write Suspend to Read**
  - **Block Erase Suspend to Write**
  - **Block Erase Suspend to Read**
- **Enhanced Data Protection Features**
  - **Flexible Block Locking**
  - **User Write Protect Switch**
- **ETOX™ V Nonvolatile Flash Technology**
- **100,000 Erase Cycles per Block**
- **64-Kword Blocks**

Intel's Series 100 Flash Memory Miniature Card offers a small form factor, low cost, removable solid-state storage solution for consumer applications. Some of these applications include digital audio recorders, digital cameras, wireless communications, and hand-held PCs. Manufactured with Intel's FlashFile™ memory, this card takes advantage of a revolutionary architecture that provides innovative capabilities, automated write/erase algorithms, reliable operation and very high read/write performance.

September 1996

Order Number: 290581-002

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ADVANCE INFORMATION

REVISION HISTORY

Number	Item
-001	Original version
-002	Added Section 8.5, Preformatted for FTL Modified test conditions for V_{OL} Modified test conditions for V_{OH} Modified Vcc Standby Current for 4 Mbyte cards Added JEDEC ID Tuple to the CIS Corrected references to Byte Writes as Word Writes

1.0 SCOPE OF DOCUMENT

This datasheet provides a card architecture overview, AC and DC characteristics and command definitions.

2.0 PRODUCT OVERVIEW

The 2- and 4-Mbyte flash memory cards each contain a flash memory array that consists of two or four 28F008SC (1-Mbyte) TSOP memory devices, respectively. Each 28F008SC contains 16 distinct, individually-erasable, 64-Kbyte blocks. Therefore, the 2- and 4-Mbyte cards contain 32 and 64 independently-erasable blocks.

At the device level, internal algorithm automation allows execution of write and erase operations using a two-write command sequence in the same way as the flash memory in the Series 2 or Value Series 100 cards. The automated write/erase algorithms ensure that data is reliably written in the least amount of time.

3.0 SERIES 100 MINIATURE CARD ARCHITECTURE OVERVIEW

The Series 100 Miniature Card is a simple array of flash devices in a Miniature Card form factor. This card offers a low-cost, small form factor, removable memory solution at 2- and 4-Mbyte densities. Two 28F008SC devices in parallel provide the lower and upper bytes for a 16-bit access. The Attribute Information Structure (AIS) for the Series 100 Miniature Card is stored in Block 0 of the flash memory to reduce the attribute memory cost overhead of an EEPROM or ASIC.

3.1 Card Pinout and Signal Description

The Miniature Card Specification provides the system interface for the Series 100 Miniature Card. The detailed specifications for this interface is described in the Miniature Card Specification.

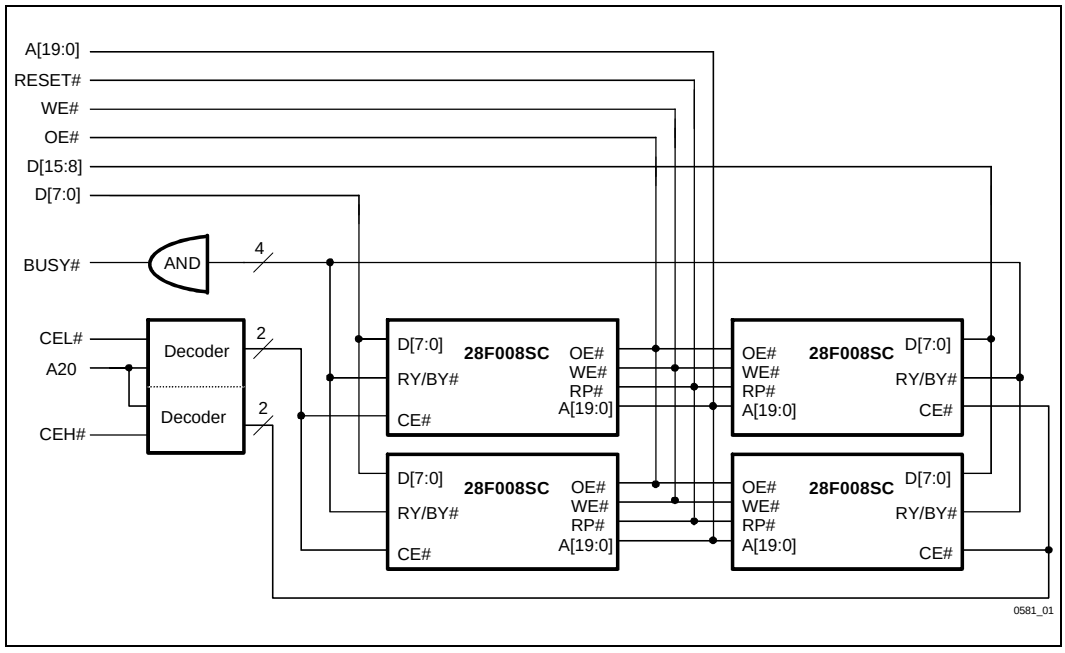


Figure 1. Flash Memory Card Block Diagram Showing Major Functional Elements

Table 1. Series 100 Miniature Card Interface Signals

Pad #	Signal Name	Pad #	Signal Name	Pad #	Signal Name
1	A_{18}	21	D_{12}	41	A_4
2	A_{16}	22	D_{10}	42	CEL#
3	A_{14}	23	D_9	43	A_1
4	VCCR(1)	24	D_0	44	CASL#(1)
5	CEH#	25	D_2	45	CASH#(1)
6	A_{11}	26	D_4	46	CD#
7	A_9	27	RFU	47	A_{21}(1)
8	A_8	28	D_7	48	BUSY#
9	A_6	29	SDA(1)	49	WE#
10	A_5	30	SCL(1)	50	D_{14}
11	A_3	31	A_{19}	51	RFU(1,2)
12	A_2	32	A_{17}	52	D_{11}
13	A_0	33	A_{15}	53	VS2#(1)
14	RAS#(1)	34	A_{13}	54	D_8
15	A_{24}(1)	35	A_{12}	55	D_1
16	A_{23}(1)	36	RESET#	56	D_3
17	A_{22}(1)	37	A_{10}	57	D_5
18	OE#	38	VS1#	58	D_6
19	D_{15}	39	A_7	59	RFU(1,2)
20	D_{13}	40	BS8#(1)	60	A_{20}(3)

NOTES:

1. These signals make no internal connection into the card.
2. Reserved pins must not be driven by the host. They should be left floating.
3. A_{20} is only decoded on the 4-Mbyte card.

Table 2. Series 100 Miniature Card Power/Insertion Signals

Signal #	Signal Name
61	GND
62	CINS#
63	V_{CC}

Table 3. Series 100 Miniature Card Interface Signal Description

Symbol	Type	Name and Function
A_0–A_{24}	INPUT	**ADDRESS INPUTS:** Addresses A_0 through A_{24} enable direct addressing of up to 64 MB of memory on the card. The memory will wrap at the card density boundary. The system should NOT try to access memory beyond the card's density, since the upper addresses are not decoded.
D_0–D_{15}	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** D_0 through D_{15} constitute the bi-directional data bus. D_{15} is the most significant bit.
CEL#, CEH#	INPUT	**CARD ENABLE LOW & HIGH:** CEL# enables accesses on the low byte of the data bus $D_{0–7}$. CEH# enables accesses on the high byte of the data bus $D_{8–15}$. Both CEL# and CEH# are active low signals. A 16-bit host must always assert both CEL# and CEH#.
OE#	INPUT	**OUTPUT ENABLE:** Active low signal, enables read data from the memory card.
WE#	INPUT	**WRITE ENABLE:** Active low signal, enables write data to the memory card.
BUSY#	OUTPUT	**BUSY:** Active low signal, indicates the status of internally timed erase or write activities. A high output indicates the memory card is ready to accept another command.
CD#	OUTPUT	**CARD DETECT:** Active low signal, provides for card insertion detection. CD# connects to ground internally on the memory card, and will be forced low when the CD# interface signal connects to the host.
RESET#	INPUT	**RESET:** Active low input signal, resets the device's command user interface and places the card into a deep power-down mode. The host must drive this signal.
VS1#, VS2#	OUTPUT	**VOLTAGE SENSE:** Notifies the host socket of the card's V_{CC} requirements. VS_1 is grounded and VS_2 is left **open** to indicate a 3.3V capable card has been inserted.
RFU	-	**RESERVED FOR FUTURE USE**

Table 4. Series 100 Miniature Card Power/Insertion Signal Description

Symbol	Type	Name and Function
CINS#	OUTPUT	**CARD INSERTION DETECT:** This signal provides for early card insertion detection. CINS# connects to ground internally on the memory card, and will be forced low when the power/insertion signals connect to the host.
V_{CC}	-	**CARD POWER SUPPLY:** 3.3V or 5V
GND	-	**GROUND**

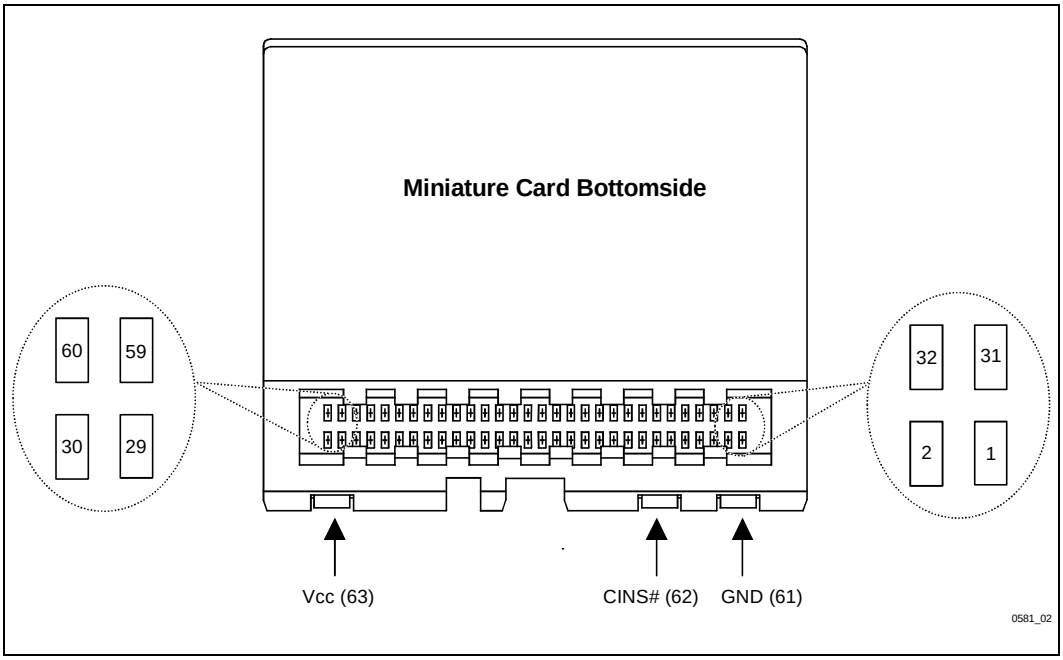


Figure 2. Card Interface Signal Assignment

4.0 28F008SC CONTROL LOGIC

4.1 Bus Operations

The host executes read, write and erase operations by issuing the appropriate command to the flash device's Command User Interface (CUI). The CUI serves as the interface between the host processor and internal operation of the flash device. These commands can be issued to the CUI using standard microprocessor bus cycles.

4.1.1 READ ARRAY

The host enables reads from the card by writing the appropriate read command to the CUI. The 28F008SC automatically resets to read array mode upon initial device power-up, or after reset. CEL#, CEH#, and OE# must be logically active to obtain 16 data bits at the outputs. The Card Enables (CEL# and CEH#) are used to select the addressed devices. Output Enable (OE#) is the data input/output (D_0–D_{15}) direction control, and when active, drives data from the selected memory onto the data bus. WE# must be driven to V_{IH} during a read access.

4.1.2 OUTPUT DISABLE

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Outputs (D_0–D_{15}) are placed in a high-impedance state.

4.1.3 STANDBY

CEL# and CEH# at a logic-high level (V_{IH}) places the card in standby mode. Standby operation disables much of the card's circuitry and substantially reduces device power consumption. The outputs (D_0–D_{15}) are placed in a high-impedance state independent of the status of OE#. If the host deselects the card during a write or erase, the card continues to function and consume normal active power until the operation completes.

4.1.4 DEEP POWER-DOWN

RESET# at V_{IL} initiates the deep power-down mode.

During reads, an active RESET# deselects the memory, places output drivers in a high-impedance state, and turns off all internal circuits. RESET# must be held low for a minimum of 100 ns. After returning from deep power-down, the host must wait before initial memory access outputs are valid, as determined by t_{PHQV}. After this wake-up interval, the host can resume normal operations to the card. Card reset forces the CUI to reset to read array mode and sets the status register to 80H.

During block erase, byte write, or lock-bit configuration modes, an active RESET# will abort the operation. BUSY# remains low until the reset operation completes. Memory contents being altered are no longer valid; the data may be partially erased or written. The host must wait after RESET# goes to logic-high (V_{IH}) before it can write another command, as determined by t_{PHWL}.

It is important to assert RESET# to the card during a system reset. When a host comes out of reset, it may require the ability to immediately execute code from the card. If a CPU reset occurs without a card reset, the host will not be able to read from the card if that card is in a different mode when the system reset occurs. For example, if an end-user initiates a host reset when the card is in read status register mode, the host will attempt to read code from the card, but will actually read status register data. Intel's Series 100 Miniature Card allows proper card reset following a system reset through the use of the RESET# input. System RESET# circuitry can reset the host CPU in addition to the card.

4.1.5 READ IDENTIFIER CODES OPERATION

The read identifier codes operation outputs the manufacturer code, device code, and block lock configuration codes (for each block), see Figure 3. Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The block lock codes identify locked and unlocked blocks.

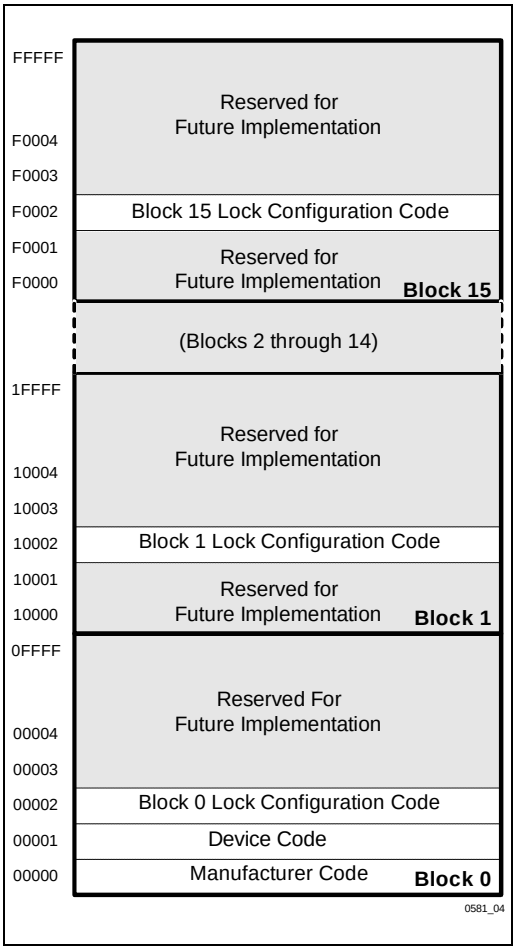


Figure 3. Device Identifier Code Memory Map

4.1.6 CUI WRITES

Writes to the CUI enable reading of device data and intelligent identifiers. They also control inspection and clearing of the Status Register. The contents of the interface register serves as input to the internal state machine on each component.

The CUI itself does not occupy an addressable memory location. The interface register is a latch used to store the command, address and data

information needed to execute the command. Erase Setup and Erase Confirm commands require both appropriate command data and an address within the block to be erased. The Write Setup command requires both appropriate command data and the address of the location to be written, while the Write command consists of the data to be written and the address of the location to be written.

The CUI is written by bringing WE# to a logic-low level (V_{IL}) while CE# is low. Addresses and data are latched on the rising edge of WE#. Standard microprocessor write timings are used.

When a write or erase command has been issued to the CUI, the internal Write State Machine (WSM) becomes busy and will not be ready until it has completed the operation.

4.2 SmartVoltage Technology

SmartVoltage technology provides a choice of V_{CC} at 3.3V or 5.0V. V_{CC} at 3.3V consumes approximately one-fourth the power of V_{CC} at 5.0V. However, V_{CC} at 5.0V provides the highest read performance. Internal device detection circuitry automatically configures the device.

5.0 CARD CONTROL LOGIC

5.1 Word Addressing

The Series 100 Miniature Card uses two x8 devices in parallel to form the Miniature Card x16 data bus (see Figure 1). If the host writes a command to the card, it must make sure that it writes the command to both devices in the card. For example, a component write command is 40H, so a card write command must be 4040H. This same procedure must be followed when reading from the status register. A component status register is only 8 bits and may return 80H when read. However, the card status register is 16 bits and may return 8080H.

5.2 Decode Logic

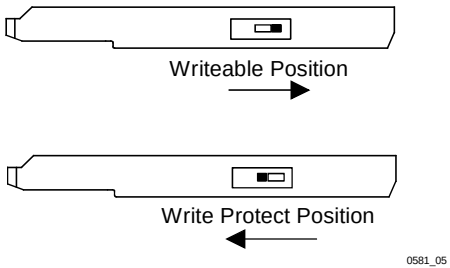
The decode logic enables the appropriate component device pair during a read or write access. Unused upper addresses for the Series 100 Miniature Card will not be decoded. The address decoding will wrap around at the card's density.

5.3 Write Protect Switch

The Series 100 Miniature Card has a write protect switch on the side of the card. When the switch is in the write protect position, the card blocks all writes to the card (see Figure 4).

NOTE

When the write protect switch is in the write protect position all writes are disabled to the flash array including all commands to the CUI.



NOTE:
The write protect switch is represented by the solid black rectangle.

Figure 4. Write Protect Switch

5.4 Data Control

As shown in Table 5, data paths and directions are selected by the Data Control logic using WE#, OE#, CEL#, and CEH# as logic inputs.

Table 5. Data Access Mode Truth Table

Mode	RESET#	CEL#	CEH#	OE#	WE#	A_0	D_{8-15}	D_{0-7}	Notes
Low Byte-Read	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	High-Z	Low(6)	1,2,3,
High Byte-Read	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	High(6)	High-Z	1,2,3,
Word-Read	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	High(6)	Low(6)	1,2,3,
Low Byte-Write	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	XXX	Low(6)	3,4,
High Byte-Write	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	High(6)	XXX	3,4,
Word-Write	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	High(6)	Low(6)	3,4,
Manufacturer ID	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	89H	89H	
Device ID	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A6H	A6H	5
Standby	V_{IH}	V_{IH}	V_{IH}	X	X	X	High-Z	High-Z	
Output Disable	V_{IH}	X	X	V_{IH}	V_{IH}	X	High-Z	High-Z	
Power-Down	V_{IL}	X	X	X	X	X	High-Z	High-Z	

NOTES:

1. Refer to DC Characteristics.
2. X can be V_{IL} or V_{IH} for control signals and address.
3. BUSY# is V_{OL} when the WSM is executing internal byte write or block erase algorithms. It is V_{OH} when the WSM is not busy, in erase suspend mode, or deep power-down mode.
4. Refer to Table 6 for valid D_{IN} during a write operation.
5. The device code can be A6H, A7H or AAH. Software should check for all three cases for compatibility with future cards.
6. High indicates high byte data, low indicates low byte data.

6.0 COMMAND DEFINITIONS

Device operations are selected by writing specific commands into the Command User Interface. Table 6 defines the 28F008SC commands.

NOTE:

When the write protect switch is in the write protect position all writes are disabled to the flash array including commands to the CUI.

6.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the card defaults to read array mode. The host can also read by writing the Read Array command. The device remains enabled for reads until the host writes another valid command. Once the internal WSM has started a block erase, byte write or lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation. However, the host can suspend the WSM using an Erase Suspend or Byte Write Suspend command.

Table 6. Command Definitions(6)

Command	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
			Oper(1)	Addr(2)	Data(3)	Oper(1)	Addr(2)	Data(3)
Read Array/Reset	1		Write	X	FFFFH			
Read Identifier Codes	≥ 2	4	Write	X	9090H	Read	IA	ID
Read Status Register	2		Write	X	7070H	Read	X	SRD
Clear Status Register	1		Write	X	5050H			
Block Erase	2		Write	BA	2020H	Write	BA	D0D0H
Word Write	2	5	Write	WA	4040H or 1010H	Write	WA	WD
Block Erase and Byte Write Suspend	1		Write	X	B0B0H			
Block Erase and Byte Write Resume	1		Write	X	D0D0H			
Set Block Lock-Bit	2		Write	BA	6060H	Write	BA	0101H
Clear Block Lock-Bits	2		Write	X	6060H	Write	X	D0D0H

NOTES:

1. Bus operations are defined in Table 5.
2. X = Any valid address within the device.
   IA = Identifier Code Address: see Figure 3.
   BA = Address within the block being erased or locked.
   WA = Address of memory location to be written.
3. SRD = Data read from status register. See Table 8 for a description of the status register bits.
   WD = Data to be written at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
   ID = Data read from identifier codes.
4. Following the Read Identifier Codes command, read operations access manufacturer, device, block lock, and master lock codes. See Section 6.2 for read identifier code data.
5. Either 40H or 10H are recognized by the WSM as the byte write setup.
6. Commands other than those shown above are reserved by Intel for future device implementations and should not be used.

6.2 Read Identifier Codes Command

The host initiates the identifier code operation by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 3 retrieve the manufacturer, device and block lock configuration codes (see Table 7 for identifier code data). To terminate the operation, write another valid command. Although Table 7 lists the device code as A6A6, this family of products could also have device codes A7A7 or AAAA. Host software should check for all three cases for compatibility with future cards.

Table 7. Identifier Codes

Code	Address	Data (2)
Manufacture Code	00000	8989
Device Code	00001	A6A6
Block Lock Configuration	X0002(1)	
• Block is Unlocked		$D_{0,8}$ = 0
• Block is Locked		$D_{0,8}$ = 1
• Reserved for Future Use		$D_{1\text{-}7,\ 9\text{-}15}$

NOTES:

1. X selects the specific block lock configuration code to be read. See Figure 3 for the device identifier code memory map.
2. The addresses listed are word addresses and store 16 bits of data. See Section 4.3 for more information on word addressing.

6.3 Read Status Register Command

The 28F008SC components on the Series 100 Miniature Card each contain a Status Register which may be read to determine when a write, block erase, or lock bit configuration is complete, and whether that operation completed successfully (see Table 8). The host may read the Status Register at any time by writing the Read Status Register command to the CUI. After writing this command, all subsequent read operations output data from the Status Register, until the host writes another valid command to the CUI. The flash components latch the contents of the Status Register on the falling edge of OE# or CE#, whichever occurs first. OE# or CE# must be toggled to V_{IH} before further reads to update the Status Register latch.

NOTE:

The Miniature Card arranges two 28F008SC devices in parallel to form a x16 bus. Both status registers need to be checked when determining the status of a x16 erase/write operation. See Section 4.3 for more information on word addressing.

6.4 Clear Status Register Command

The WSM sets the Erase Status and Write Status bits to “1”s and they can only be reset by the Clear Status Register command. The WSM sets these bits to “1” when a write or erase operation has failed. The host can issue additional write and erase commands to the CUI without clearing the status register. This allows a system to write a sequence of bytes before checking the write status bit. However, if an error has occurred the system will not know which write in the sequence has failed. To clear the Status Register, the Clear Status Register command (5050H) is written to the CUI.

NOTE:

If V_{PP} has not been turned on, the WSM sets the V_{PP} status bit. However, the Series 100 Miniature Card ties V_{PP} and V_{CC} on the 28F008SC devices together so if V_{CC} is on then V_{PP} will also be on. If for some reason the WSM sets the V_{PP} Status bit, the host **must** clear the status register before it attempts further writes or block erases.

6.5 Block Erase Command

The host executes an erase command one block at a time using a two-cycle command. The host writes a block erase setup command first, followed by a block erase confirm command. These two commands require appropriate sequencing and an address within the block to complete (erase changes all block data to FFH). The WSM handles block preconditioning, erase, and verify internally (invisible to the system). After the host writes the two-cycle block erase sequence, the device automatically outputs status register data when read. The CPU can detect block erase completion by analyzing the output data of the BUSY# signal or status register bit SR.7.

When the block erase completes, status register bit SR.5 should be checked. If a block erase error is detected, the host should clear the status register before system software attempts corrective actions. The CUI remains in read status register mode until the host issues a new command.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in the WSM setting status register bits SR.4 and SR.5 to "1." Successful block erase requires that the corresponding block lock-bit is not set. If the host attempts a block erase when the corresponding block lock-bit is set, the WSM will set SR.1 and SR.5 to "1."

6.6 Word Write Command

The host executes a word write by a two-cycle command sequence. The host writes word write setup (standard 4040H or alternate 1010H) first, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the word write and write verify algorithms internally. After the host writes the word write sequence, the device automatically outputs status register data when read. The CPU can detect the completion of the byte write event by analyzing the BUSY# pin or status register bit SR.7.

When the WSM completes the word write, the host should check status register bit SR.4. If the host detects a write error, it should clear the status register. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Successful word writes requires that the corresponding block lock-bit is not set. If the host attempts a write when the corresponding block lock-bit is set, the WSM will set SR.1 and SR.4 "1."

6.7 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or write data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. After the host writes the Block Erase Suspend command, the host should then write the Read Status Register command. Polling status register bits SR.7 and SR.6 can determine when the WSM suspends the block erase operation (both will be set to "1"). BUSY# will also transition to V_{OH}. Specification t_{WHRH2} defines the block erase suspend latency. It is also possible that the block erase completes before the device has an opportunity to suspend. The host should also check for this condition.

After the block erase has been suspended, the host can issue a read array command or a word write command to any block except the one that has been suspended. Using the Word Write Suspend command (see Section 6.8), a word write operation can also be suspended. During a word write operation with block erase suspended, status register bit SR.7 will return to "0" and the BUSY# output will transition to V_{OL}. However, SR.6 will remain "1" to indicate block erase suspend status. The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After the host writes a Block Erase Resume command to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and BUSY# will return to V_{OL}. After the host writes the Erase Resume command, the device automatically outputs status register data when read. Block erase cannot resume until word write operations initiated during block erase suspend have completed.

6.8 Word Write Suspend Command

The Word Write Suspend command allows word write interruption to read data in other flash memory locations. Once the word write process starts, writing the Word Write Suspend command requests that the WSM suspend the word write sequence at a predetermined point in the algorithm. After the host writes the Word Write Suspend command, it should write the Read Status Register command. Polling status register bits SR.7 and SR.2 can determine when the WSM suspends the byte write operation (both will be set to "1"). BUSY# will also transition to V_{OH}. Specification t_{WHRH1} defines the word write suspend latency. It is also possible that the word write completes before the device has an opportunity to suspend. The host should also check for this condition.

After the word write has been suspended, the host can write the Read Array command to read data from any location except the suspended location. The only other valid commands while word write is suspended are Read Status Register and Word Write Resume. After the host writes a Word Write Resume to the CUI, the WSM will continue the word write process. Status register bits SR.2 and SR.7 will automatically clear and BUSY# will return to V_{OL}. After the host writes the Word Write Resume command, the device automatically outputs status register data when read.

6.9 Set Block Lock-Bit Command

The host can enable a flexible block locking and unlocking scheme using the Set Block Lock-Bit command. This command enables the host to lock individual blocks within the flash array. The block lock-bits gate program and erase operations.

The host sets the block lock-bit using a two-cycle command sequence. The host writes the set block lock-bit setup command along with the appropriate block or device address. This command is followed by the set block lock-bit confirm command (and an address within the block to be locked). The WSM controls the set lock-bit algorithm. After the host completes the command sequence, the card automatically outputs status register data when read. The CPU can detect the completion of the set lock-bit event by analyzing the BUSY# pin output or status register bit SR.7.

When the WSM completes the set lock-bit operation, the host should check status register bit SR.4. If the host detects an error it should clear the status register. The CUI will remain in read status register mode until the host issues a new command.

This two-step sequence of set-up followed by execution ensures that the host does not accidentally set the lock-bits. An invalid Set Block Lock-Bit command will result in the WSM setting status register bits SR.4 and SR.5 to “1.”

6.10 Clear Block Lock-Bits Command

The host clears all set block lock-bits in parallel using the Clear Block Lock-Bits command. The host is free to clear block lock-bits using the Clear Block Lock-Bits command

The host executes the clear block lock-bits operation using a two-cycle command sequence. The host must first issue a Clear Block Lock-Bits setup command. This command is followed by a confirm command. After the host completes the two-cycle command sequence, the device automatically outputs status register data when read. The CPU can detect completion of the clear block lock-bits event by analyzing the BUSY# pin output or status register bit SR.7.

When the WSM completes the operation, the host should check status register bit SR.5. If the host detects a clear block lock-bit error, the host should clear the status register. The CUI will remain in read status register mode until the host issues another command.

This two-step sequence of set-up followed by execution ensures that the host does not accidentally clear block lock-bits. An invalid Clear Block Lock-Bits command sequence will result in the WSM setting status register bits SR.4 and SR.5 to “1.”

If a clear block lock-bits operation is aborted due to V_{CC} transitioning out of valid range or RESET# active transition, block lock-bit values are left in an undetermined state. The host must repeat the clear block lock-bits command to initialize block lock-bit contents to known values.

Table 8. Status Register Definition

WSMS	ESS	ECLBS	BWSLBS	VPPS	BWSS	DPS	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy

SR.6 = ERASE SUSPEND STATUS
1 = Block Erase Suspended
0 = Block Erase in Progress/Completed

SR.5 = ERASE AND CLEAR LOCK-BITS STATUS
1 = Error in Block Erasure or Clear Lock-Bits
0 = Successful Block Erase or Clear Lock-Bits

SR.4 = BYTE WRITE AND SET LOCK-BIT STATUS
1 = Error in Byte Write or Set Master/Block Lock-Bit
0 = Successful Byte Write or Set Master/Block Lock Bit

SR.3 = V_{PP} STATUS
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

SR.2 = BYTE WRITE SUSPEND STATUS
1 = Byte Write Suspended
0 = Byte Write in Progress/Completed

SR.1 = DEVICE PROTECT STATUS
1 = Block Lock-Bit and/or RESET# Lock Detected, Operation Abort
0 = Unlock

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS

NOTES:

Check BUSY# or SR.7 to determine block erase, byte write, or lock-bit configuration completion. SR.6-0 are invalid while SR.7 = "0."

If both SR.5 and SR.4 are "1"s after a block erase or lock-bit configuration attempt, an improper command sequence was entered.

SR.3 indicates the V_{PP} status. However, the Miniature Card internally ties V_{PP} to V_{CC} so this bit should not be set to "1." If for some reason this bit is set, the host should write the Clear Status Register command.

SR.1 does not provide a continuous indication of master and block lock-bit values. The WSM interrogates the master lock-bit, block lock-bit, and RESET# only after Block Erase, Byte Write, or Lock-Bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set, master lock-bit is set, and/or RESET# is not V_{HH}. Reading the block lock and master lock configuration codes after writing the Read Identifier Codes command indicates master and block lock-bit status.

SR.0 is reserved for future use and should be masked out when polling the status register.

7.0 CARD ATTRIBUTE INFORMATION

The Card Attribute Information consists of the Miniature Card's Attribute Information Structure (AIS) as well as the PC Card's Card Information Structure (CIS). These two structures co-exist for compatibility with both industry standards. This allows the Series 100 Miniature Card to function in both PC Card and Miniature Card environments.

The Card Attribute Information data for the Series 100 Miniature Card is found in Section 7.3. For more information on the description of these structures refer to the appropriate specification.

CAUTION:

The Card Attribute Information data is located in Block 0. This information is not write protected and should not be erased by the system software if this information is needed for card recognition.

7.1 Card Information Structure

The CIS begins at address 0000H (device tuple) of the card's memory. The CIS data resides only in the low byte of the word. It contains a variable length chain of data blocks (tuples) that conform to a basic format. See Table 9 for the CIS memory map.

7.2 Attribute Information Structure

The AIS begins at address 0010H (identifier byte) of the card's memory. The AIS data resides only in the low byte of the word. It contains a fixed list of data information that ends at address 00FFH. See Table 10 for the AIS memory map.

NOTE:

All addresses listed in Table 9 and 10 are **WORD** addresses.

Table 9. CIS Memory Map

Tuple Name	Description	Tuple Code	Address Location
CISTPL_DEVICE	Device Information	01H	0H - 04H
CISTPL_NULL	Null (Ignore)	00H	05H - 0DH
CISTPL_MINI	Miniature Card AIS (Vendor Unique)	80H	0EH - FFH
CISTPL_DEVICEGEO	Device Geometry Information	1EH	100H - 107H
CISTPL_MANFID	Manufacturer Identification String	20H	108H - 10DH
CISTPL_FUNCID	Function Class Identification	21H	10EH - 111H
CISTPL_LONGLINK_C	Longlink to Common Memory	12H	112H - 117H
CISTPL_VERS_1	Level 1 Version/Product Information	15H	118H - 167H
CISTPL_DEVICE_OC	Other Operating Conditions Device Info.	1CH	168H - 16CH
CISTPL_JEDEC_C	JEDEC ID	18H	16DH - 170H
CISTPL_END	The End-of-Chain Tuple	FFH	171H - 172H

Table 10. AIS Memory Map

AIS Section	Description	Address Location
Identification Data	Identifies Card Type	10H - 3FH
Compatibility Data	Describes Attributes of Card	40H - 4FH
Not Used	Reserved for Future Use	50H - FFH

7.3 Card Attribute Information Data

Address	Values	Description
00H	01H	**CISTPL_DEVICE**
01H	03H	TPL_LINK
02H	54H	FLASH = 100 ns
03H	06H	CARD SIZE: 2 MB
	0EH	CARD SIZE: 4 MB
04H	FFH	END OF DEVICE
05H - 0DH	00H	NULL
0EH	80H	**CISTPL_MIN**
0FH	F0H	TPL_LINK
10H	99H	Identifier
11H	10H	Rev 1.0 Compliant
12H	F2H	2 MB AIS Checksum
	EFH	4 MB AIS Checksum
13H	49H	Manufacturer Name I
14H	4EH	N
15H	54H	T
16H	45H	E
17H	4CH	L
18H	20H	SPACE
19H	43H	C
1AH	4FH	O
1BH	52H	R
1CH	50H	P
1DH	4FH	O
1EH	52H	R
1FH	41H	A
20H	54H	T

Address	Values	Description
21H	49H	I
22H	4FH	O
23H	4EH	N
24H - 26H	00H	NULL
27H	53H	Card Name S
28H	45H	E
29H	52H	R
2AH	49H	I
2BH	45H	E
2CH	53H	S
2DH	20H	SPACE
2EH	31H	1
2FH	30H	0
30H	30H	0
31H	20H	SPACE
32H	43H	C
33H	41H	A
34H	52H	R
35H	44H	D
36H - 3AH	00H	NULL
3BH	01H	1 Technology Device
3CH - 3FH	00H	Reserved Space Set to 00H
40H	00H	Flash
41H	89H	Device JEDEC Manufacturer ID

Address	Values	Description
42H	A6H	Device JEDEC Component ID
43H	02H	2 MB
	04H	4 MB
44H	00H	no x.x V Accesses
45H	15H	150 ns 3.3 V Access Time
46H	10H	100 ns 5.0 V Access Time
47H	00H	no x.x V Accesses
48H	25H	20 mA read/50 mA write @ 3.3 V
49H	46H	40 mA read/60 mA write @ 5.0 V
4AH	01H	100 µA standby - 2 MB
	02H	200 µA standby - 4 MB
4BH - 4FH	00H	Reserved
50 - FF	00H	NULL / Not Used
100H	1EH	**CISTPL_DEVICEGEO**
101H	06H	TPL_LINK
102H	02H	DGTPL_BUS
103H	11H	DGTPL_EBS
104H	01H	DGTPL_RBS
105H	01H	DGTPL_WBS
106H	03H	DGTPL_PART = 1
107H	01H	FLASH DEVICE INTERLEAVE
108H	20H	**CISTPL_MANFID**
109H	04H	TPL_LINK
10AH	89H	TPLMID_MANF: LSB

Address	Values	Description
10BH	00H	TPLMID_MANF: MSB
10CH	03H	2 MB - 100 ns
	13H	4 MB - 100 ns
10DH	85H	TPLMID_CARD MSB
10EH	21H	**CISTPL_FUNCID**
10FH	02H	TPL_LINK
110H	01H	TPLFID_FUNCTION : Memory
111H	00H	TPLFID_SYSINIT
112H	12H	**CISTPL_LONGLINK_C**
113H	04H	TPL_LINK
114H	00H	LOWEST BYTE
115H	00H	MID BYTE
116H	02H	MID BYTE
117H	00H	HIGHEST BYTE
118H	15H	**CISTPL_VERS1**
119H	4EH	TPL_LINK
11AH	05H	TPLLV1_MAJOR
11BH	00H	TPLLV1_MINOR
11CH	49H	TPLLV1_INFO I
11DH	6EH	n
11EH	74H	t
11FH	65H	e
120H	6CH	l
121H	00H	END TEXT
122H	53H	S
123H	45H	E
124H	52H	R

Address	Values	Description
125H	49H	I
126H	45H	E
127H	53H	S
128H	20H	SPACE
129H	31H	1
12AH	30H	0
12BH	30H	0
12CH	20H	SPACE
12DH	46H	F
12EH	4CH	L
12FH	41H	A
130H	53H	S
131H	48H	H
132H	20H	SPACE
133H	4DH	M
134H	49H	I
135H	4EH	N
136H	49H	I
137H	41H	A
138H	54H	T
139H	55H	U
13AH	52H	R
13BH	45H	E
13CH	20H	SPACE
13DH	43H	C
13EH	41H	A
13FH	52H	R
140H	44H	D

Address	Values	Description
141H	00H	END TEXT
142H	30H	2 MB
	30H	4 MB
143H	32H	2 MB
	34H	4 MB
144H	20H	SPACE
145H	00H	END TEXT
146H	43H	C
147H	4FH	O
148H	50H	P
149H	59H	Y
14AH	52H	R
14BH	49H	I
14CH	47H	G
14DH	48H	H
14EH	54H	T
14FH	20H	SPACE
150H	49H	I
151H	4EH	N
152H	54H	T
153H	45H	E
154H	4CH	L
155H	20H	SPACE
156H	43H	C
157H	4FH	O
158H	52H	R
159H	50H	P
15AH	4FH	O
15BH	52H	R

Address	Values	Description
15CH	41H	A
15DH	54H	T
15EH	49H	I
15FH	4FH	O
160H	4EH	N
161H	20H	SPACE
162H	31H	1
163H	39H	9
164H	39H	9
165H	36H	6
166H	00H	END TEXT
167H	FFH	END OF LIST
168H	1CH	**CISTPL_DEVICE_OC**
169H	03H	TPL_LINK
16AH	02H	3.3V Operation
16BH	53H	150 ns Access Time
16CH	06H	CARD SIZE: 2 MB
	0EH	CARD SIZE: 4 MB
16DH	18H	**CISTPL_JEDEC_C**
16EH	02H	TPL_LINK
16FH	89H	MANUFACTURER ID
170H	A6H	DEVICE ID
171EH	FFH	**CISTPL_END**
172FH	00H	INVALID ADDRESS

8.0 SYSTEM DESIGN CONSIDERATIONS

8.1 Power Supply Decoupling

Flash memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current issues: standby, active and transient current peaks which are produced by rising and falling edges of CEL# and CEH#. The capacitive and inductive loads on the card and internal flash memory device pairs determine the magnitudes of these peaks.

The host system should also have a 4.7 µF electrolytic capacitor between V_{CC} and GND as close to the connector as possible. The bulk capacitance overcome voltage slumps caused by printed-circuit-board trace inductance, and supply charge to the smaller capacitors as needed.

8.2 Power-Up/Down Protection

The Miniature Card specified socket properly sequences the power supplies to the flash memory card via power/insertion signals that connect before the interface signals.

Each device in the memory card is designed to offer protection against accidental erasure or writing, caused by spurious system-level signals that may exist during power transitions. The card will power-up into the read state.

A system designer must guard against active writes for V_{CC} voltages above V_{LKO} (2.0V). Since WE# and CEH#/CEL# must be active for a command write, driving either to V_{IH} will inhibit writes. The card provides 100 KΩ pull-up resistors on CEH# and CEL# to provide some protection against spurious writes.

The two-step command sequence for a write provides additional protection against accidental writes to the card.

8.3 BUSY# and Byte Write/Block Erase Polling

BUSY# is a CMOS output that provides a hardware method of detecting byte write and block erase completion. BUSY# transitions low a maximum of 100 ns after the host issues a Write or Erase command sequence. BUSY# returns to V_{OH} when the WSM has finished executing the internal algorithm or the host suspends the current operation.

BUSY# can be connected to the interrupt input of the system CPU or controller. It is active at all times. BUSY# is also V_{OH} when the device is in erase suspend or deep power-down modes.

8.4 V_{CC}, RESET# Transitions and the Command/Status Registers

RESET# transitions to V_{IL} during write and block erase also aborts the operations. Data is partially altered in either case, and the command sequence must be repeated after normal operation is restored. Device power-off, or RESET# transitioning to V_{IL}, clears the Status Register to initial value 100000XX.

Systems that do not support RESET# or Power-Down functionality must tie the RESET# signal to V_{CC}.

The CUI latches commands issued by system software and is not altered by CE# transitions or WSM actions. The CUI defaults to read array mode upon power-up, exit from deep power-down, or after V_{CC} transitions below V_{LKO}.

After write or block erase is complete, the CUI must be reset to read array mode via the Read Array command, if access to the memory array is desired.

8.5 Preformatted for FTL

FTL is an industry-standard file format for storing data in flash memory. In order for FTL host software to read and write data files to the Miniature Card, the card must first be formatted for FTL. Formatting includes adding FTL structures on every block boundary of the flash array. All Miniature Cards come preprogrammed with appropriate FTL structures on the card.

9.0 ELECTRICAL SPECIFICATIONS

NOTICE: This datasheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design

9.1 Absolute Maximum Ratings*

Commercial Operating Temperature

during Read, Block Erase, Word Write, and Lock-Bit Configuration ..... 0°C to +60°C(1)

Temperature under Bias.....–10°C to +70°C

Storage Temperature .....–30°C to +70°C

Voltage on Any Pin (except V_{CC})..–2.0V to +7.0V(2)

V_{CC} Supply Voltage.....–2.0V to +7.0V(2)

Output Short Circuit Current..... 100 mA(3)

** WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may effect device reliability.*

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is –0.5V on input/output pins and –0.2V on V_{CC}. During transitions, this level may undershoot to –2.0V for periods <20 ns. Maximum DC voltage on input/output signals and V_{CC} is V_{CC} +0.5V which, during transitions, may overshoot to V_{CC} +2.0V for periods <20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

9.2 Operating Conditions

Symbol	Parameter	Notes	Min	Max	Unit	Test Condition
T_A	Operating Temperature		0	+60	°C	Ambient Temperature
V_{CC1}	V_{CC} Supply Voltage (3.3V ± 0.3V)		3.0	3.6	V	
V_{CC2}	V_{CC} Supply Voltage (5V ± 5%)		4.75	5.25	V	

9.2.1 CAPACITANCE(1)

Symbol	Parameter	Typical	Maximum	Unit	Condition
C_{IN}	Input Capacitance	2 MB = 12 4 MB = 24	2 MB = 16 4 MB = 32	pF	V_{IN} = 0.0V
C_{OUT}	Output Capacitance	2 MB = 16 4 MB = 16	2 MB = 24 4 MB = 24	pF	V_{OUT} = 0.0V

NOTES:

1. Sampled, not 100% tested.

9.2.2 AC INPUT/OUTPUT TEST CONDITIONS

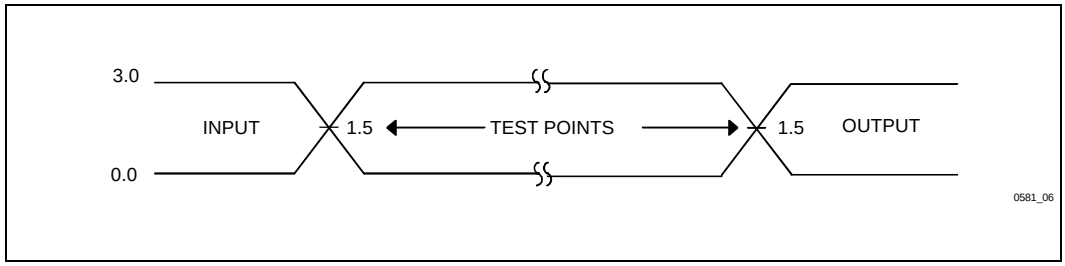


Figure 5. Transient Input/Output Reference Waveform for V_{CC} = 3.3V ± 0.3V and V_{CC} = 5V ± 5% (Standard Testing Configuration)

9.3 DC Characteristics [6]

DC Characteristics

Sym	Parameter	Notes	V_{CC} = 3.3V		V_{CC} = 5V		Unit	Test Conditions
			Typ	Max	Typ	Max		
I_{LI}	Input Load Current	1,4		1		2	µA	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1		1		20	µA	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1,3	90[7] 220[8]	240[7] 520[8]	80[7] 200[8]	240[7] 520[8]	µA	$V_{CC} = V_{CC}$ Max CEL# = CEH# = RESET# = V_{CC} ± 0.2V
I_{CCD}	V_{CC} Deep Power-Down Current	1,3		30[7] 100[8]		30[7] 100[8]	µA	RESET# = GND ± 0.2V I_{OUT} (RY/BY#) = 0 mA
I_{CCR}	V_{CC} Read Current	1,3,5	20	25	35	70		$V_{CC} = V_{CC}$ Max, CEL#/CEH# = GND, f = 5 MHz (3.3V), f = 8 MHz (5.0V), I_{OUT} = 0 mA
I_{CCW}	V_{CC} Word Write or Set Lock-Bit Current	1,4	45	115	60	150	mA	
I_{CCE}	V_{CC} Block Erase or Clear Lock-Bit Current	1,4	45	75	60	100	mA	
I_{CCWS} I_{CCES}	V_{CC} Word Write or Block Erase Suspend Current	1,2	6	12	10	20	mA	CEL# = CEH# = V_{IH}

NOTES:

1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (packages and speeds). Contact Intel's Application Support Hotline or your local sales office for information about typical specifications.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or byte written while in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. CMOS inputs are either V_{CC} ± 0.2V or GND ± 0.2V.
4. Exceptions: With V_{IN} = GND, the leakage current on CEL#, CEH# will be <50 µA each due to internal pull-up resistors.
5. Automatic Power Savings (APS) reduces typical I_{CCR} to 2 mA at 5V V_{CC} and 6 mA at 3.3V V_{CC} in static operation (addresses not switching).
6. All values are based on word accesses. Values for byte accesses are 50% of the specification listed.
7. These values are specific to 2-Mbyte cards.
8. These values are specific to 4-Mbyte cards.

DC Characteristics

Sym	Parameter	Notes	V_{CC} = 3.3V		V_{CC} = 5V		Unit	Test Conditions
			Min	Max	Min	Max		
V_{IL}	Input Low Voltage		–0.5	0.8	–0.5	0.8	V	
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 0.5	2.0	0.7 V_{CC}	V	
V_{OL}	Output Low Voltage			0.1 V_{CC}		0.1 V_{CC}	V	V_{CC} = V_{CC} Min I_{OL} = 4.0 mA @ 5V I_{OL} = 2 mA @ 3.3V
V_{OH}	Output High Voltage		0.9 V_{CC}		0.9 V_{CC}		V	V_{CC} = V_{CC} Min I_{OH} = –1 mA
V_{LKO}	V_{CC} Lockout Voltage		2.0		2.0		V	

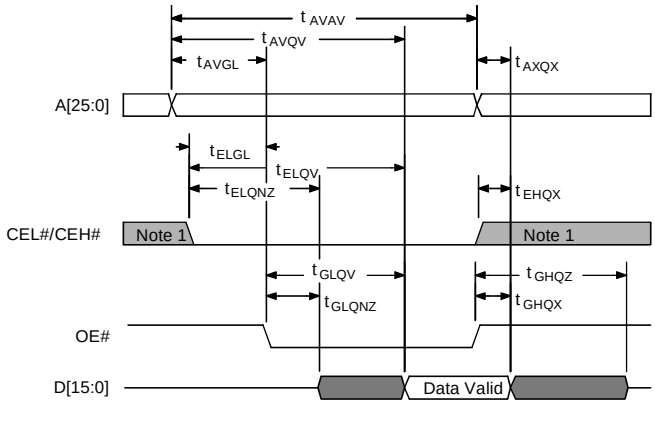
9.4 AC Characteristics

AC timing diagrams and characteristics are guaranteed to meet or exceed the Miniature Card Specification.

9.4.1 READ OPERATIONS

Parameter	IEEE Symbol	5V Min	5V Max	3.3V Min	3.3V Max	Unit
Read Cycle Time	t_{AVAV}	100		150		ns
Address Access Time	t_{AVQV}		100		150	ns
CE# Access Time	t_{ELQV}		100		150	ns
OE# Access Time	t_{GLQV}		40		50	ns
Output Disable Time from OE# Inactive	t_{GHQZ}		10		20	ns
Output Enable Time from OE# Active(1)	t_{GLQNZ}	5		5		ns
Output Enable Time from CE# Active(1)	t_{ELQNZ}	5		5		ns
Data Hold from Address, CE#, or OE# Change (Whichever Occurs First)	t_{AXQX}	0		0		ns
CE# Setup Time to OE# Active	t_{ELGL}	0		0		ns
Address Setup Time to OE# Active	t_{AVGL}	0		0		ns
RESET# High to Output Delay	t_{PHQV}		400		600	ns

NOTES:
1. Sampled, not 100% tested.

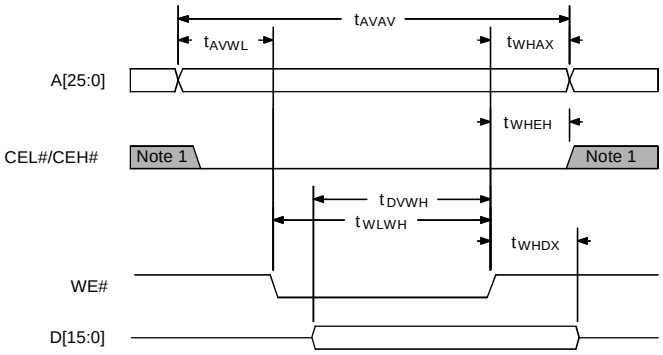


NOTE:
1. Shaded region may be high or low.

Figure 6. AC Waveforms for Read Operations

9.4.2 WRITE OPERATIONS

Parameter	IEEE Symbol	5V Min	5V Max	3.3V Min	3.3V Max	Unit
Write Cycle Time	t_{AVAV}	100		150		ns
Address Access Time	t_{AVQV}		100		150	ns
CE# Access Time	t_{ELQV}		100		150	ns
WE# Pulse Width	t_{WLWH}	40		50		ns
Address Setup Time to WE# Active	t_{AVWL}	0		0		ns
Data Setup Time to WE# Inactive	t_{DVWH}	40		50		ns
Data Hold Time from WE# Inactive	t_{WHDX}	5		5		ns
Address Hold Time from WE# Inactive	t_{WHAX}	5		5		ns
CE# Hold Time from WE# Inactive	t_{WHEH}	10		10		ns
RESET# High to WE# Active	t_{PHWL}	1		1		µs



NOTE:
1. Shaded region may be high or low.

Figure 7. AC Waveforms for Write Operations

9.4.3 POWER-UP TIMING

Symbol	Parameter	Notes	Min	Max	Units
t_{su} (CEL#/CEH#)	CE# Setup Time		1		ms
t_{su} (RESET#)	RESET# Setup Time		1		ms
t_{pr}	V_{CC} Rising Time	1	0.1	100	ms
t_w (RESET#)	RESET# Width		1		µs

NOTE:

1. The t_{pr} is defined as a “linear waveform” in the period of 10% to 90%. Even if the waveform is not a “linear waveform,” its rising time must meet this specification.

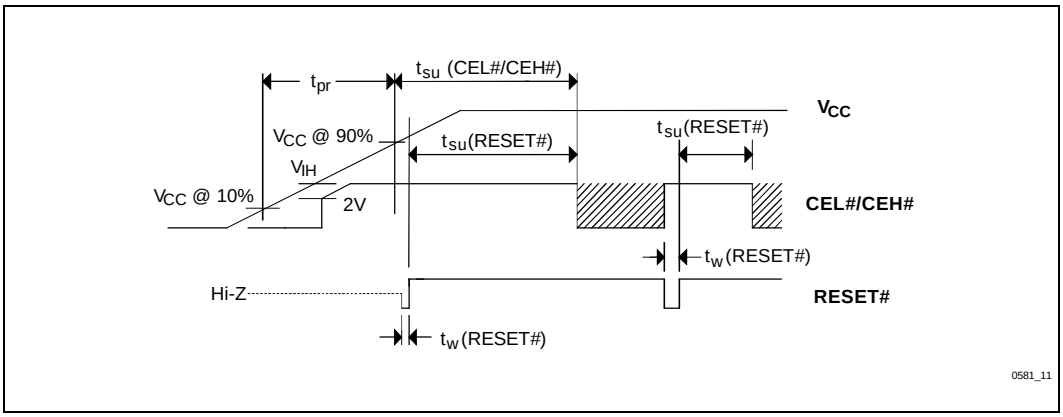


Figure 8. Power-Up Timing for Systems Supporting RESET#

10.0 ERASE AND DATA WRITE PERFORMANCE(3,4,5)

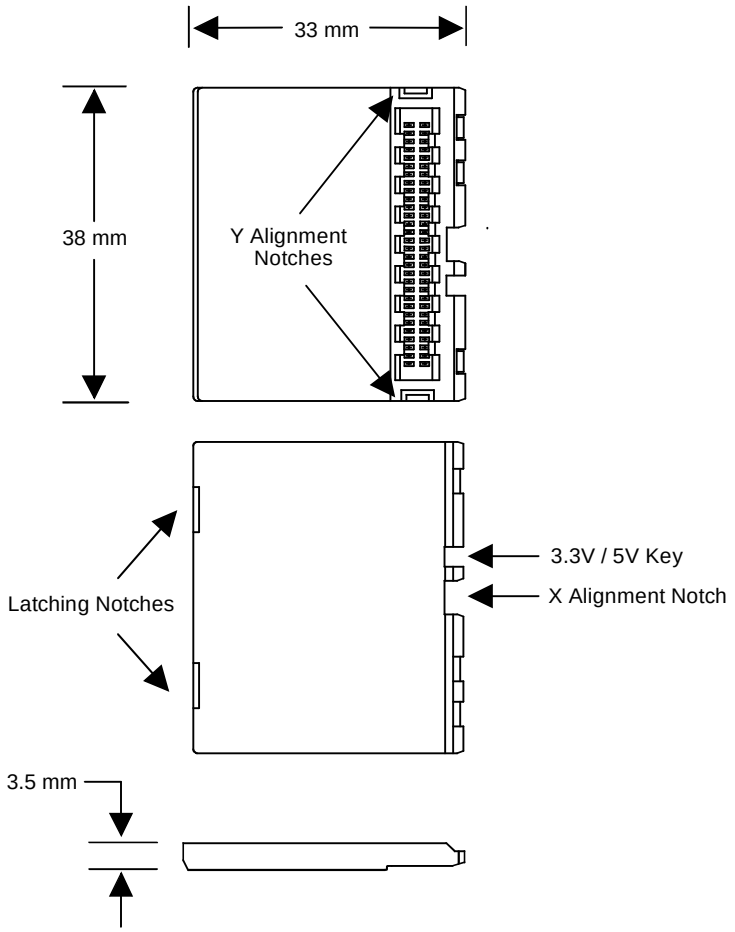
Sym	Parameter	Notes	V_{CC} = 3.3V			V_{CC} = 5.0V			Unit
			Min	Typ(1)	Max	Min	Typ(1)	Max	
t_{WHQV1} t_{EHQV1}	Word Write Time	2		17			8		µs
	Block Write Time	2		1.1			0.5		sec
t_{WHQV2} t_{EHQV2}	Block Erase Time	2		1.8			1.1		sec
t_{WHQV3} t_{EHQV3}	Set Lock-Bit Time	2		21			12		µs
t_{WHQV4} t_{EHQV4}	Clear Block Lock-Bits Time	2		1.8			1.1		sec
t_{WHRH1} t_{EHRH1}	Word Write Suspend Latency Time to Read			6	7		5	6	µs
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency Time to Read			16.2	20		9.6	12	µs

NOTES:

1. Typical values measured at T_A = +25°C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled but not 100% tested.
5. The maximum word/byte write time is the absolute maximum time it takes the write algorithm to complete. The overwhelming majority of the bits program in the typical value specified.

11.0 PACKAGING

Figure 9 shows the outside dimensions of the Series 100 Miniature Card. For complete mechanical drawings refer to the Miniature Card Specification.



NOTE:
For complete dimensions of the 3.3V/5.0V key, refer to the Miniature Card Specification.

Figure 9. Miniature Card Dimensions

APPENDIX A
ORDERING INFORMATION

iFM004A, SHXXXXX

Where:

i	= INTEL
FM	= FLASH MINIATURE CARD
004	= DENSITY IN MEGABYTES (002, 004 AVAILABLE)
A	= REVISION
SHXXXXX	= CUSTOMER IDENTIFIER

APPENDIX B
ADDITIONAL INFORMATION

RELATED INTEL INFORMATION(1,2)

Order Number	Document
290577	*28F008SC 8-Mbit (1 Mb x 8) SmartVoltage FlashFile™ Memory Datasheet*
292182	*AP-627 28F008SA and 28F008SC Software Drivers*

NOTES:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.