PRELIMINARY

VALUE SERIES 100

FLASH MEMORY CARD
2-, 4-, 8- and 16- MEGABYTES

iMC002FLSC, iMC004FLSC, iMC008FLSC, iMC016FLSC

- **Low-Cost Linear Flash Card**
- **Single Supply: 5 Volt Operation**
- **FAST Read Performance**
  - **100 ns Maximum Access Time**
- **x16 Data Interface**
- **High-Performance Random Writes**
  - **8 µs Typical Word Write**
- **Automated Program and Erase Algorithms**
  - **28F008SA Command Set**
- **State-of-the-Art 0.4 µm ETOX™ V Flash Technology**
- **100,000 Erase Cycles per Block**
- **64-Kword Blocks**
- **PC Card Standard Type 1 Form Factor**

Intel's Value Series 100 card offers the lowest cost removable solid-state storage solution for code and data storage, high-performance disk emulation, and applications in mobile PCs and dedicated embedded applications. Manufactured with Intel's FlashFile™ memory, this card takes advantage of a revolutionary architecture that provides innovative capabilities, automated program/erase algorithms, reliable operation and very high read/write performance.

The flash memory card provides the lowest cost, highest performance nonvolatile read/write solution for solid-state storage applications. These applications are enhanced further with this product's symmetrically-blocked architecture, extended MTBF, and 5 Volt operation.

The flash memory card can be used as a simple x16 linear array of flash devices. The PC Card form factor offers an industry-standard pinout, removable linear flash memory, and the ability to upgrade system memory software without changing the board layout.

December 1996

Order Number: 290546-002

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PRELIMINARY

REVISION HISTORY

Revision	Description
-001	Original
-002	Added Specifications for 16-Mbyte Card Added 16-Mbyte Tuples Added I_{CCSL} for 16-Mbyte Card Changed A_{24} from N.C. to Active Changed Interface to CMOS only–removed Table 9.3 TTL Interfacing Changed DC specification and text to reflect conversion to the 28F0xxS5 family

1.0 SCOPE OF DOCUMENT

This datasheet provides a card architecture overview, all AC and DC characteristics and command definitions.

2.0 PRODUCT OVERVIEW

The 2-, 4-, 8- or 16-Mbyte cards consist of two, four, eight or sixteen 28F008SA flash memories. All members of the 28F008SA family are made up of 64-Kbyte, individually erasable blocks. Therefore, the 2-, 4-, 8- or 16-Mbyte cards contain 32, 64, 128 or 256 independently-erasable, 64-Kbyte blocks.

When accessed as 16-bit words, the blocks appear to be 128-Kbytes. The high byte is in one 64-Kbyte block, the low byte in another. In this mode, the 2-, 4-, 8- and 16-Mbyte cards contain 16, 32, 64 or 128 independent 128-Kbyte blocks.

At the device level, internal algorithm automation allows execution of program and erase operations using a two-program command sequence. The automated program/erase algorithms ensure that data is reliably written in the least amount of time.

The memory card interface supports the PC Card Standard, supported by Personal Computer Memory Card Industry Association (PCMCIA) and Japanese Electronics Industry Development Association (JEIDA) 68-pin card format. The Value Series 100 card meets all PCMCIA/JEIDA Type 1 mechanical specifications.

3.0 VALUE SERIES 100 CARD ARCHITECTURE OVERVIEW

A Value Series 100 card is an array of flash memory devices in a PC Card form factor. Pairs of 28F008SA devices, connected in parallel, provide lower and upper bytes of a 16-bit access.

Typical flash memory components only support a single operation at a time. Only one block in a 28F008SA can erased, or only one location programmed, at a time. Since a Value Series 100 contains multiple devices, it is possible to perform multiple concurrent operations in the card. A location in one component can be read while a location in another component is being programmed. Using a card in this way is discouraged, because future versions of the card may use different components.

Today's Value Series 100 cards are based on a 1-Mbyte component, so an 8-Mbyte card will have eight components and could perform up to eight concurrent operations. When 8-Mbyte components become available, that 8-Mbyte card will have only one component. If an algorithm required multiple components because it performed multiple, concurrent operations, that algorithm will not be compatible with the new card. Incidentally, all DC characteristics assume that only one operation is being performed at a time, and all other components on the card are in stand-by.

In the future, the Value Series may use higher capacity memory devices. Therefore, algorithms that are based on a particular organization may not be compatible with these newer, more cost-effective cards.

The Card information Structure (CIS) for the Value Series 100 card is stored in Block 0 of the flash memory to reduce the attribute memory cost overhead of an EEPROM or ASIC. In embedded applications, a CIS may not be required by the system and the entire memory array can be used by the system.

3.1 Card Pinout and Pin Description

The 68-pin PC Card format provides the system interface for the Value Series 100 card (see Tables 1 and 2). The detailed specifications for this interface are described in the PC Card Standard Specification. The Value Series 100 card product family conforms to the pinout requirements of previous PCMCIA Versions Release 1.0, Release 2.0 and Release 2.01 and the PC Card Standard.

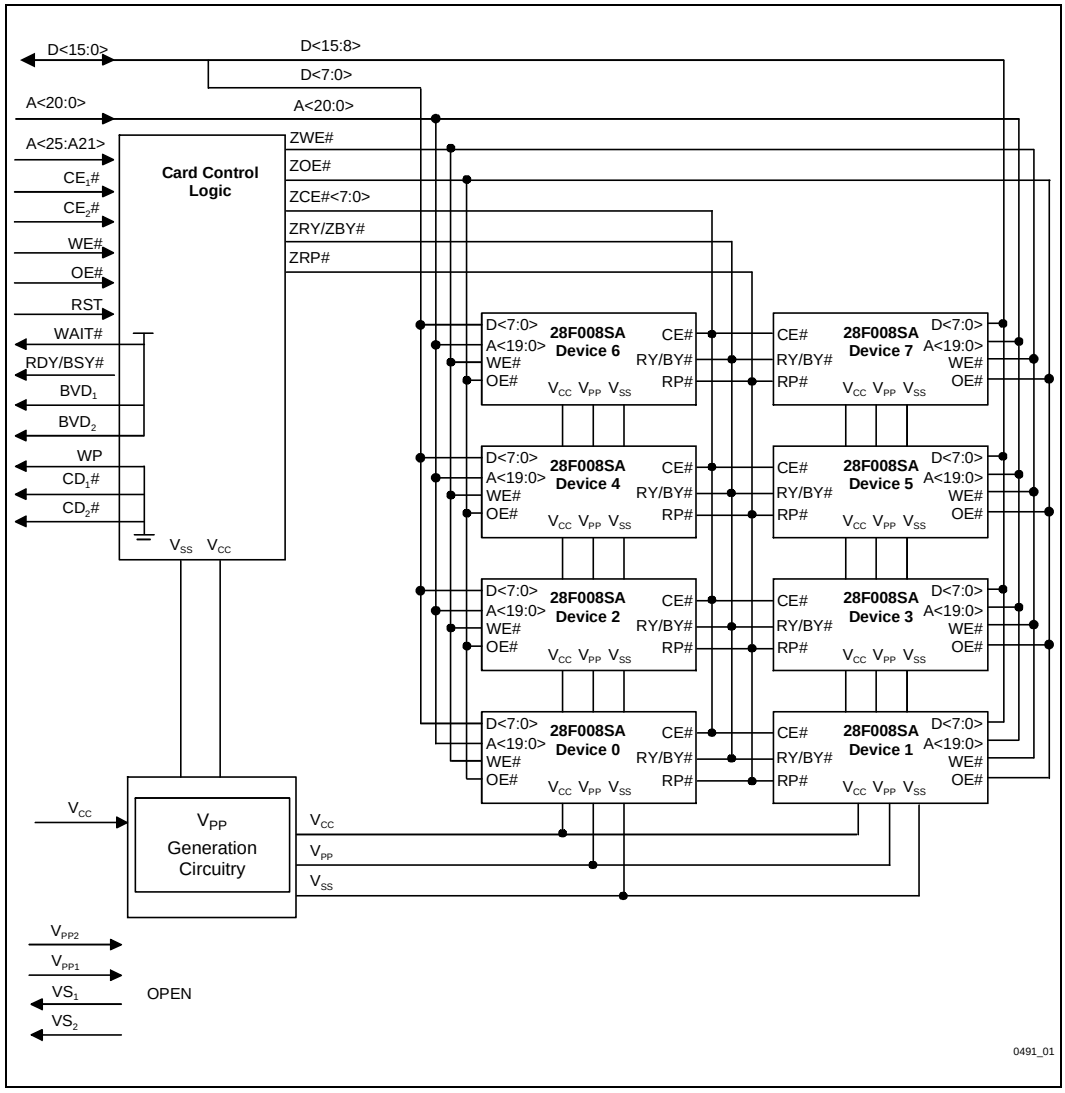


Figure 1. 8-Mbyte Flash Memory Card Block Diagram Showing Major Functional Elements

Table 1. Value Series 100 Card Signals

Pin	Signal	I/O	Function	Active	Pin	Signal	I/O	Function	Active
1	GND		Ground		27	A_2	I	Address Bit 2	
2	DQ_3	I/O	Data Bit 3		28	A_1	I	Address Bit 1	
3	DQ_4	I/O	Data Bit 4		29	A_0	I	Address Bit 0	
4	DQ_5	I/O	Data Bit 5		30	DQ_0	I/O	Data Bit 0	
5	DQ_6	I/O	Data Bit 6		31	DQ_1	I/O	Data Bit 1	
6	DQ_7	I/O	Data Bit 7		32	DQ_2	I/O	Data Bit 2	
7	CE_1#	I	Card Enable 1	LOW	33	WP	O	Write Protect	HIGH
8	A_{10}	I	Address Bit 10		34	GND		Ground	
9	OE#	I	Output Enable	LOW	35	GND		Ground	
10	A_{11}	I	Address Bit 11		36	CD_1#	O	Card Detect 1	LOW
11	A_9	I	Address Bit 9		37	DQ_{11}	I/O	Data Bit 11	
12	A_8	I	Address Bit 8		38	DQ_{12}	I/O	Data Bit 12	
13	A_{13}	I	Address Bit 13		39	DQ_{13}	I/O	Data Bit 13	
14	A_{14}	I	Address Bit 14		40	DQ_{14}	I/O	Data Bit 14	
15	WE#	I	Write Enable	LOW	41	DQ_{15}	I/O	Data Bit 15	
16	RDY/BSY#	O	Ready/Busy	LOW	42	CE_2#	I	Card Enable 2	LOW
17	V_{CC}		Supply Voltage		43	VS_1	O	Voltage Sense 1	N.C.
18	V_{PP1}		Supply Voltage	N.C.	44	RFU		Reserved	
19	A_{16}	I	Address Bit 16		45	RFU		Reserved	
20	A_{15}	I	Address Bit 15		46	A_{17}	I	Address Bit 17	
21	A_{12}	I	Address Bit 12		47	A_{18}	I	Address Bit 18	
22	A_7	I	Address Bit 7		48	A_{19}	I	Address Bit 19	
23	A_6	I	Address Bit 6		49	A_{20}	I	Address Bit 20	
24	A_5	I	Address Bit 5		50	A_{21}	I	Address Bit 21	
25	A_4	I	Address Bit 4		51	V_{CC}		Supply Voltage	
26	A_3	I	Address Bit 3		52	V_{PP2}		Supply Voltage	N.C.

Table 1. Value Series 100 Card Signals (Continued)

Pin	Signal	I/O	Function	Active
53	A_{22}	I	Address Bit 22	
54	A_{23}	I	Address Bit 23	
55	A_{24}	I	Address Bit 24	
56	A_{25}	I	Address Bit 25	N.C.
57	VS_2	O	Voltage Sense 2	N.C.
58	RST	I	Reset	HIGH
59	WAIT#	O	Extend Bus Cycle	LOW
60	RFU		Reserved	

Pin	Signal	I/O	Function	Active
61	REG#	I	Attribute Memory Select	
62	BVD_2	O	Battery Voltage Detect 2	
63	BVD_1	O	Battery Voltage Detect 1	
64	DQ_8	I/O	Data Bit 8	
65	DQ_9	I/O	Data Bit 9	
66	DQ_{10}	I/O	Data Bit 10	
67	CD_2#	O	Card Detect 2	LOW
68	GND		Ground	

Table 2. Value Series 100 Card Signal Description

Symbol	Type	Name and Function
A_0–A_{25}	INPUT	**ADDRESS INPUTS:** A_0 through A_{25} enable direct addressing of up to 64 MB of memory on the card. Signal A_0 is not decoded since the card is x16 only. The memory will wrap at the card density boundary. The system should NOT try to access memory beyond the card's density, since the upper addresses are not decoded.
DQ_0–DQ_{15}	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** DQ_0 through DQ_{15} constitute the bi-directional data bus. DQ_{15} is the most significant bit.
CE_1#, CE_2#	INPUT	**CARD ENABLE 1 & 2:** CE_1# enables EVEN byte accesses on $D_{0–7}$, CE_2# enables ODD byte accesses on $D_{8–15}$. Cannot access Odd Bytes on $D_{0–7}$.
OE#	INPUT	**OUTPUT ENABLE:** Active low signal enabling read data from the memory card.
WE#	INPUT	**WRITE ENABLE:** Active low signal gating write data to the memory card.
RDY/BSY#	OUTPUT	**READY/BUSY OUTPUT:** Indicates status of internally timed erase or program activities. A high output indicates the memory card is ready to accept accesses.
CD_1#, CD_2#	OUTPUT	**CARD DETECT 1 & 2:** These signals provide for card insertion detection. The signals are connected to ground internally on the memory card, and will be forced low whenever a card is placed in the socket. The host socket interface circuitry shall supply 10K or larger pull-up resistors on these signal pins.
WP	OUTPUT	**WRITE PROTECT:** This signal is pulled LOW for PC Card Standard compatibility. The flash memory card has no WP signal functionality.
V_{PP1},V_{PP2}	N.C.	**PROGRAM/ERASE POWER SUPPLY:** These power signals are not connected for the 5V-only card.
V_{CC}		**CARD POWER SUPPLY:** 5.0V for all internal circuitry.
GND		**GROUND** for all internal circuitry.
REG#	INPUT	**REGISTER SELECT:** The memory card has no separate attribute memory. The CIS is located in common memory. REG# is unconnected on the card.
RST	INPUT	**RESET:** Active high signal for placing card in Power-On Default State. RESET can be used as a POWER-DOWN signal for the memory array.
WAIT#	OUTPUT	**WAIT:** (Extended Bus Cycle) This signal is pulled high for compatibility.
BVD_1, BVD_2	OUTPUT	**BATTERY VOLTAGE DETECT:** These signals are pulled high to maintain SRAM card compatibility.
VS_1, VS_2	OUTPUT	**VOLTAGE SENSE:** Notifies the host socket of the card's V_{CC} requirements. VS_1 and VS_2 are OPEN to indicate a 5V, 16-bit card has been inserted.
RFU		**RESERVED FOR FUTURE USE**
N.C.		**NO INTERNAL CONNECTION TO CARD** pin may be driven or left floating.

4.0 CARD CONTROL LOGIC

4.1 Bus Operations

Flash memory reads, erases and programs are performed using bus cycles to or from the flash memory that conform to standard microprocessor bus cycles.

4.1.1 READ

The components on the Value Series 100 card have three read modes: read memory array, read intelligent identifier or read Status Register; they are enabled by writing the appropriate read mode command to the Command User Interface (CUI). The 28F008SA automatically resets to read array mode upon initial device power-up, or after reset.

The 28F008SA has four control pins, two of which must be logically active to obtain data at the outputs. Chip Enables ($CE_{1,2}$#) are the device selection control, and, when active, enable the selected memory device. Output Enable (OE#) is the data input/output (DQ_0–DQ_{15}) direction control, and, when active, drives data from the selected memory onto the I/O bus. WE# must be driven to V_{IH} during a read access.

4.1.2 OUTPUT DISABLE

With OE# and WE# at a logic-high level (V_{IH}), the device outputs are disabled. Output (DQ_0–DQ_{15}) are placed in a high-impedance state.

4.1.3 STANDBY

$CE_{1,2}$# at a logic-high level (V_{IH}) places the card in standby mode. Standby operation disables much of the card's circuitry and substantially reduces device power consumption. The outputs (DQ_0–DQ_{15}) are placed in a high-impedance state independent of the status of OE#. If the card is de-selected during program or block erase, the card will continue functioning and consuming normal active power until the operation completes.

4.1.4 INTELLIGENT IDENTIFIER OPERATION

The intelligent identifier operation outputs the manufacturer code, 89H, and the device code: A2H, A6H or AAH. The table below lists the device and capacity for each device code.

Device Code	Device Type	Component Capacity
A2H	28F008SA	1 MB
A6H	28F008S5	1 MB
AAH	28F016S5	2 MB

A system should recognize all three codes in order to support current cards, based on the 28F008SA and newer cards based on the 28F0xxS5 family.

The manufacturer and device codes are read via the CUI. Following a write of 9090H to the CUI, a read from address location 0000H outputs the manufacturer code (8989H). A read from address 0002H outputs the device code: A2A2H, A6A6H, or AAAAH.

Future cards may incorporate devices that implement the Common Flash Interface (CFI). This standard supports forward and backward compatibility between flash memories. New algorithms should first determine if the card is CFI compliant, and if it is not, then read the intelligent identifiers.

4.1.5 WRITE

Writes to the CUI enable reading of device data and intelligent identifiers. They also control inspection and clearing of the Status Register. The contents of the interface register serves as input to the internal state machine on each component.

The CUI itself does not occupy an addressable memory location. The interface register is a latch used to store the command, address and data information needed to execute the command. Erase Setup and Erase Confirm commands require both appropriate command data and an address within the block to be erased. The Program Setup command requires both appropriate command data and the address of the location to be written, while the Program command consists of the data to be written and the address of the location to be written.

The CUI is written by bringing WE# to a logic-low level (V_{IL}) while CE# is low. Addresses and data are latched on the rising edge of WE#. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the AC Waveforms for Write Operations, Figure 14, for specific timing parameters.

4.2 Address Decode Logic

The address decode logic selects which components device pair is enabled during a read or write access. Unused upper addresses for the Value Series 100 card will not be decoded. The address decoding will wrap around at the card's density.

The Value Series 100 card does not have a separate attribute memory space and REG# is not included in the address decode logic. REG# accesses will result in a read/write to the common memory flash array.

4.3 Data Control

As shown in Table 3, data paths and directions are selected by the Data Control logic using WE#, OE#, CE_1#, and CE_2# as logic inputs. The Data Control logic selects any of the PCMCIA word-wide, EVEN-byte and ODD-byte modes for either reads or writes to common memory.

NOTE:

This card has a x16 interface. The **odd** byte **cannot** be accessed on the lower data path (D_{0-7}). A_0 is not decoded.

Table 3. Data Access Mode Truth Table

Mode	RESET	CE_2#	CE_1#	OE#	WE#	A_1	V_{PP}	D_{8-15}	D_{0-7}	Notes
Even Byte-Read	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	High-Z	Even	1,2
Odd Byte-Read	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	X	Odd	High-Z	1,2
Word-Read	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	Odd	Even	1,2
Even Byte-Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	XXX	Even	3
Odd Byte-Write	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	X	Odd	XXX	3
Word-Write	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	X	Odd	Even	3
Manufacturer ID	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	89H	89H	
Device ID	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	A6H	A6H	4
Standby	V_{IL}	V_{IH}	V_{IH}	X	X	X	X	High-Z	High-Z	
Output Disable	V_{IL}	X	X	V_{IH}	V_{IH}	X	X	High-Z	High-Z	
Power-Down	V_{IH}	X	X	X	X	X	X	High-Z	High-Z	

NOTES:

1. Refer to DC Characteristics.
2. X can be V_{IL} or V_{IH} for control pins and address.
3. Refer to Table 4 for valid D_{IN} during a program operation.
4. The device code can be A6H or AAH. Software should check for all three cases for compatibility with future cards.

5.0 COMMAND DEFINITIONS

Device operations are selected by writing specific commands into the Command User Interface. Table 4 defines the 28F008SA commands.

5.1 Read Array Command (FFFFH)

Upon initial device power-up, and after reset, the 28F008SA defaults to read array mode. This operation is also initiated by writing FFFFH into the CUI on the component. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the CUI contents are altered by issuing a valid command. Once the internal WSM has started a byte program or block erase operation, the device will not recognize the Read Array command until the WSM has completed its operation.

5.2 Intelligent Identifier Command (9090H)

The 28F008SA contains an intelligent identifier operation, initiated by writing 9090H into the CUI. Following the command write, a ready cycle from address 00000H retrieves the manufacturer code of 8989H. A read cycle from address 00002H returns the device code of A2A2H, A6A6H, or AAAAH. To terminate the operation, it is necessary to write another valid command into the register.

Table 4. 28F008SA-Compatible Mode Command Bus Definitions

Command	First Bus Cycle				Second Bus Cycle			
	R/W	Addr	Data		R/W	Addr	Data	
			Byte	Word			Byte	Word
Read Array	W	DA	FFH	FFFFH	R	DA	AD	AD
Intelligent Identifier	W	DA	90H	9090H	R	IA	ID	ID
Read Status Register	W	DA	70H	7070H	R	DA	SRD	SRD
Clear Status Register	W	DA	50H	5050H				
Program	W	PA	40H	4040H	W	PA	PD	PD
Program (Alternate)	W	PA	10H	1010H	W	PA	PD	PD
Block Erase/Confirm	W	BA	20H	2020H	W	BA	D0H	D0D0H
Erase Suspend/Resume	W	DA	B0H	B0B0H	W	DA	D0H	D0D0H

ADDRESSES:

DA	Device Address
BA	Block Address
IA	Identifier Address
PA	Program Address

DATA:

AD	Array Data
SRD	Status Reg. Data
ID	Identifier Data
PD	Program Data

5.3 Read Status Register Command (7070H)

The 28F008SA components on the Value Series 100 card each contain a Status Register which may be read to determine when a program or block erase operation is complete, and whether that operation completed successfully. The Status Register may be read at any time by writing the Read Status Register command (7070H) to the CUI. After writing this command, all subsequent read operations output data from the Status Register, until another valid command is written to the CUI. The contents of the Status Register are latched on the falling edge of OE# or CE#, whichever occurs first. OE# or CE# must be toggled to V_{IH} before further reads to update the Status Register latch.

NOTE:

Two 28F008SA devices are used in parallel to form a x16 operation. Both status registers need to be checked when determining the status of a x16 erase/program operation.

5.4 Clear Status Register Command (5050H)

The Erase Status and Program Status bits are set to “1”s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 5). By allowing system software to control the resetting of these bits, several operations may be performed (such as cumulatively writing several bytes or erasing multiple blocks in sequence). The Status Register may then be polled to determine if an error occurred during that sequence. This Status Register functionality adds flexibility to the way the device may be used.

Additionally, the V_{PP} Status bit (SR.3) MUST be reset by system software before further writes or block erases are attempted. To clear the Status Register, the Clear Status Register command (50H) is written to the CUI.

Table 5. Status Register Definition

WSMS	ESS	ES	PS	VPPS	R	R	R
7	6	5	4	3	2	1	0

	NOTES:
SR.7 = WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy	RDY/BSY# or the Write State Machine Status bit must first be checked to determine byte write or block erase completion, before the Byte Write or Erase Status bit are checked for success.
SR.6 = ERASE SUSPEND STATUS 1 = Erase Suspended 0 = Erase in Progress/Completed	
SR.5 = ERASE STATUS 1 = Error in Block Erasure 0 = Successful Block Erase	If the Program *and* Erase Status bits are set to "1"s during a block erase attempt, an improper command sequence was entered. Attempt the operation again.
SR.4 = PROGRAM STATUS 1 = Error in Program 0 = Successful Program	If V_{PP} low status is detected, the Status Register must be cleared before another program or block erase operation is attempted.
SR.3 = V_{PP} STATUS 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK	The V_{PP} Status bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates the V_{PP} level only after the Program or Block Erase command sequence have been entered and informs the system if V_{PP} has not been switched on.
SR.2-SR.0 = RESERVED FOR FUTURE ENHANCEMENTS.	These bits are reserved for future use and should be masked out when polling the Status Register

5.5 Erase Setup/Erase Confirm Commands (2020H, D0D0H)

Erase is executed one block at a time, initiated by the two-cycle command sequence. An Erase Setup command (2020H) is first written to the CUI, followed by the Erase Confirm command (D0D0H). These commands require both appropriate sequencing and an address within the block to be erased to FFFFH. Block preconditioning, erase and verify are all handled internally by the WSM, invisible to the system. After the two-command erase sequence is written to it, the 28F008SA automatically outputs Status Register data when read (see Figure 8, Block Erase Flowchart). The CPUcan detect the completion of the erase event by analyzing the output data of the RDY/BSY# pin, or the WSM Status bit of the Status Register. When erase is completed, the Erase Status bit should be checked. If erase error is detected the Status Register should be cleared. The CUI remains in read Status Register mode until further commands are issued to it.

5.6 Erase Suspend/Erase Resume Commands (B0B0H, D0D0H)

The Erase Suspend command allows block erase interruption in order to read data from another block of memory. Once the erase process starts, writing the Erase Suspend command (B0B0H) to the CUI requests that the WSM suspend the erase sequences at a predetermined point in the erase algorithm. The 28F008SA continues to output Status Register data when read, after the Erase Suspend command is written to it. Polling the WSM Status and Erase Suspend Status bits will determine when the erase operation has been suspended (both will be set to "1"). RDY/BSY# will also transition to V_{OH}.

At this point, a Read Array command can be written to the CUI to read data from blocks other than that which is suspended. The only other valid commands, at this time, are Read Status Register (7070H) and Erase Resume (D0D0H), at which time the WSM will continue with the erase process. The Erase Suspend Status and WSM Status bits of the Status Register will automatically cleared and the RDY/BSY# will return to V_{OL}. After the Erase Resume command is written to it, the 28F008SA automatically outputs Status Register data when read.

5.7 Program Commands (4040H or 1010H)

The Program command is executed by a two-command sequence. The Program Setup command (4040H or 1010H) is written to the CUI, followed by a second write specifying the address and data (latched on the rising edge of WE#) to be programmed.

The WSM then takes over, controlling the program and program verify algorithms internally. After the two-command write sequence is written to it, the 28F008SA automatically outputs Status Register data when read. The CPU can detect the completion of the program event by analyzing the output of the RDY/BSY# pin, or the WSM Status bit of the Status Register. Only the Read Status Register command is valid while program is active.

When program is complete, the Program Status bit should be checked. If program error is detected, the Status Register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully program to "0"s. The CUI remains in read Status Register mode until further commands are issued to it.

6.0 PC CARD INFORMATION STRUCTURE

The Card Information Structure (CIS) begins at address 00000000H of the card's Common Memory Plane in the EVEN byte locations. It contains a variable length chain of data blocks (tuples) that conform to a basic format (Table 6). The CIS of the Value Series 100 card is found in Table 7.

CAUTION:

The CIS data in Block 0 is not write protected and should not be erased by the system software if the CIS is needed for card recognition.

Table 6. PC Card Tuple Format

Bytes	Data
0	Tuple Code: CISTPL_xxx. The tuple code 0FFH indicates no more tuples in the list.
1	Tuple Link: TPL_LINK. Link to the next tuple in the list. This can be viewed as the number of additional bytes in tuple, excluding this byte. A link field of zero indicates an empty tuple body. A link field containing 0FFH indicates the last tuple in the list.
2-n	Bytes specific to this tuple.

Table 7. Value Series 100 Card Tuples

Address	Value	Description
00H	01H	**CISTPL_DEVICE**
02H	03H	TPL_LINK
04H	54H	FLASH = 100 ns
06H	06H	CARD SIZE: 2 MB
	0EH	4 MB
	1EH	8 MB
	3EH	16 MB
08H	FFH	END OF DEVICE
0AH	1EH	**CISTPL DEVICEGEO**
0CH	06H	TPL_LINK
0EH	02H	DGTPL_BUS
10H	11H	DGTPL_EBS
12H	01H	DGTPL_RBS
14H	01H	DGTPL_WBS
16H	03H	DGTPL_PART = 1
18H	01H	FLASH DEVICE INTERLEAVE
1AH	20H	**CISTPL_MANFID**
1CH	04H	TPL_LINK (04H)
1EH	89H	TPLMID_MANF: LSB
20H	00H	TPLMID_MANF: MSB
22H	03H	2 MB - 100 ns
	13H	4 MB - 100 ns
	23H	8 MB - 100 ns
	33H	16 MB - 100 ns
24H	85H	TPLMID_CARD MSB
26H	21H	**CISTPL_FUNCID**
28H	02H	TPL_LINK
2AH	01H	TPLFID_FUNCTION : Memory
2CH	00H	TPLFID_SYSINIT
2EH	12H	**CISTPL_LONGLINK_C**
30H	04H	TPL_LINK
32H	00H	LOWEST BYTE
34H	00H	
36H	02H	
38H	00H	HIGHEST BYTE
3AH	15H	**CISTPL_VERS1**
3CH	40H	TPL_LINK
3EH	05H	TPLLV1_MAJOR
40H	00H	TPLLV1_MINOR
42H	69H	TPLLV1_INFO i
44H	6EH	n
46H	74H	t
48H	65H	e
4AH	6CH	l
4CH	00H	END TEXT
4EH	56H	V
50H	41H	A
52H	4CH	L

Address	Value	Description
54H	55H	U
56H	45H	E
58H	20H	SPACE
5AH	53H	S
5CH	45H	E
5EH	52H	R
60H	49H	I
62H	45H	E
64H	53H	S
66H	20H	SPACE
68H	31H	1
6AH	30H	0
6CH	30H	0
6EH	20H	SPACE
70H	00H	END TEXT
72H	30H 30H 30H 31H	2 MB 4 MB 8 MB 16 MB
74H	32H 34H 38H 36H	2 MB 4 MB 8 MB 16 MB
76H	20H	SPACE
78H	00H	END TEXT
7AH	43H	C
7CH	4FH	O
7EH	50H	P
80H	59H	Y
82H	52H	R
84H	49H	I
86H	47H	G
88H	48H	H
8AH	54H	T

Address	Value	Description
8CH	20H	SPACE
8EH	49H	I
90H	4EH	N
92H	54H	T
94H	45H	E
96H	4CH	L
98H	20H	SPACE
9AH	43H	C
9CH	4FH	O
9EH	52H	R
A0H	50H	P
A2H	4FH	O
A4H	52H	R
A6H	41H	A
A8H	54H	T
AAH	49H	I
ACH	4FH	O
AEH	4EH	N
B0H	20H	SPACE
B2H	31H	1
B4H	39H	9
B6H	39H	9
B8H	35H	5
BAH	00H	END TEXT
BCH	FFH	END OF LIST
BEH	FFH	**CISTPL_END**
C0H	00H	INVALID ADDRESS

7.0 SYSTEM DESIGN CONSIDERATIONS

7.1 Power Supply Decoupling

Flash memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current issues: standby, active and transient current peaks which are produced by rising and falling edges of CE_1# and CE_2#. The capacitive and inductive loads on the card and internal flash memory device pairs determine the magnitudes of these peaks.

Three-line control and proper decoupling capacitor selection suppress transient voltage peaks. The Value Series 100 cards contain on-card ceramic decoupling capacitors connected between V_{CC} and GND.

The card connector should also have a 4.7 µF electrolytic capacitor between V_{CC} and GND. The bulk capacitors overcome voltage slumps caused by printed-circuit-board trace inductance, and supply charge to the smaller capacitors as needed.

7.2 Power-Up/Down Protection

The PCMCIA/JEIDA-specified socket properly sequences the power supplies to the flash memory card via shorter and longer pins.

Each device in the memory card is designed to offer protection against accidental erasure or writing, caused by spurious system-level signals that may exist during power transitions. The card will power-up into the read state.

A system designer must guard against active writes for V_{CC} voltages above V_{LKO} (2.0V). Since both WE# and CE_1# must be low for a command write, driving either to V_{IH} will inhibit writes. With its control register architecture, alteration of device contents only occurs after successful completion of the two-step command sequences.

7.3 RDY/BSY# and Program/Block Erase Polling

RDY/BSY# is a full CMOS output that provides a hardware method of detecting program and block erase completion. It transitions low time t_{WHRL} after a Program or Erase command sequence is written to a 28F008SA, and returns to V_{OH} when all the WSM has finished executing the internal algorithm.

RDY/BSY# can be connected to the interrupt input of the system CPU or controller. It is active at all times. RDY/BSY# is also V_{OH} when the device is in erase suspend or deep power-down modes.

7.4 V_{CC}, V_{PP}, RESET Transitions and the Command/Status Registers

Program and block erase completion are not guaranteed if the internally generated V_{PP} drops below V_{PPH}. If the V_{PP} Status bit of the Status Register (SR.3) is set to "1," a Clear Status Register command *must* be issued before further program/block erase attempts are allowed by the WSM. Otherwise, the Program (SR.4) or Erase Status (SR.5) bits of the Status Register will be set to "1"s, if error is detected. RESET transitions to V_{IH} during program and block erase also abort the operations. Data is partially altered in either case, and the command sequence must be repeated after normal operation is restored. Device power-off, or RESET transitions to V_{IH}, clear the Status Register to initial value 10000XXX for the upper eight bits.

The CUI latches commands, as issued by system software, and is not altered by CE# transitions, or WSM actions. Its state upon power-up, after exit from deep power-down or after V_{CC} transitions below V_{LKO}, is read array mode.

After program or block erase is complete, the CUI must be reset to read array mode via the Read Array command, if access to the memory array is desired.

8.0 ELECTRICAL SPECIFICATIONS

NOTICE: This datasheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design

8.1 Absolute Maximum Ratings*

Operating Temperature

During Read ..... 0°C to +70°C(1)

During Write ..... 0°C to +70°C(1)

Storage Temperature.....–30°C to +80°C

Voltage on Any Pin with Respect to Ground ..... –2.0V to V_{CC} +2.0V(2)

V_{CC} Supply Voltage with Respect to Ground .....–0.5V to +7.0V

** WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may effect device reliability.*

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to -2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods less than 20 ns.

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.75	5.25	V

9.0 VALUE SERIES 100 CARD DC CHARACTERISTICS

9.1 General

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
I_{LI}	Input Leakage Current	1,2		± 20	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1		± 20	µA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or GND
V_{IL}	Input Low Voltage	1	0	0.8	V	
V_{IH}	Input High Voltage	1	3.85	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage	1		0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	1	V_{CC} – 0.4	V_{CC}	V	I_{OH} = –2.0 mA
V_{LKO}	V_{CC} Erase/Program Lock Voltage	1	2.0		V	

NOTES:

1. Values are the same for byte and word wide modes for all card densities.
2. Exceptions: With V_{IN} = GND, the leakage current on CE_1#, CE_2#, OE#, and WE# will be < 500 µA due to internal pull-up resistors. With $V_{IN} = V_{CC}$, RST leakage current will be < 150 µA due to internal pull-down resistors.

9.2 CMOS Interfacing: V_{CC} = 5.0V

DC Characteristics(1)

Sym	Parameter	Density (Mbytes)	Notes	x16 Mode		Units	Test Conditions
				Typ	Max		
I_{CCR}	V_{CC} Read Current	2, 4, 8, 16			75	mA	V_{CC} = V_{CC} Max t_{CYCLE} = 100 ns
I_{CCW}	V_{CC} Program Current	2, 4, 8, 16			100	mA	
I_{CCE}	V_{CC} Erase Current	2, 4, 8, 16			100	mA	
I_{CCSL}	V_{CC} Sleep Current	2, 4, 8	2	50	160	µA	V_{CC} = V_{CC} Max Control Signals = Vcc RESET = V_{IH}
I_{CCSL}	V_{CC} Sleep Current	16	2	90	240	µA	V_{CC} = V_{CC} Max Control Signals = V_{CC} RESET = V_{IH}
I_{CCS}	V_{CC} Standby Current	2, 4, 8	2	3	10	mA	V_{CC} = V_{CC} Max Control Signals = V_{CC}

CMOS Test Conditions: V_{IL} = GND ± 0.2V, V_{IH} = V_{CC} ± 0.2V

NOTES:

1. All currents are RMS values unless otherwise specified. Typical V_{CC} = 5V, T = +25°C.
2. Control Signals: CE_1#, CE_2#, OE#, WE#.

10.0 AC CHARACTERISTICS

AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications. No delay occurs when switching between the common and attribute memory planes.

10.1 Read Operations: Common Memory

Symbol		Parameter	100 ns at 5V		Unit
JEDEC	PCMCIA		Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	100		ns
t_{AVQV}	t_a (A)	Address Access Time		100	ns
t_{ELQV}	t_a (CE)	Card Enable Access Time		100	ns
t_{GLQV}	t_a (OE)	Output Enable Access Time		50	ns
t_{EHQX}	t_{dis} (CE)	Output Disable Time from CE#		50	ns
t_{GHQZ}	t_{dis} (OE)	Output Disable Time from OE#		50	ns
t_{ELQX}	t_{en} (CE)	Output Enable Time from CE#	5		ns
t_{GLQX}	t_{en} (OE)	Output Enable Time from OE#	5		ns
t_{PHQV}		Power-Down Recovery to Output Delay. V_{CC} = 5V		530	ns

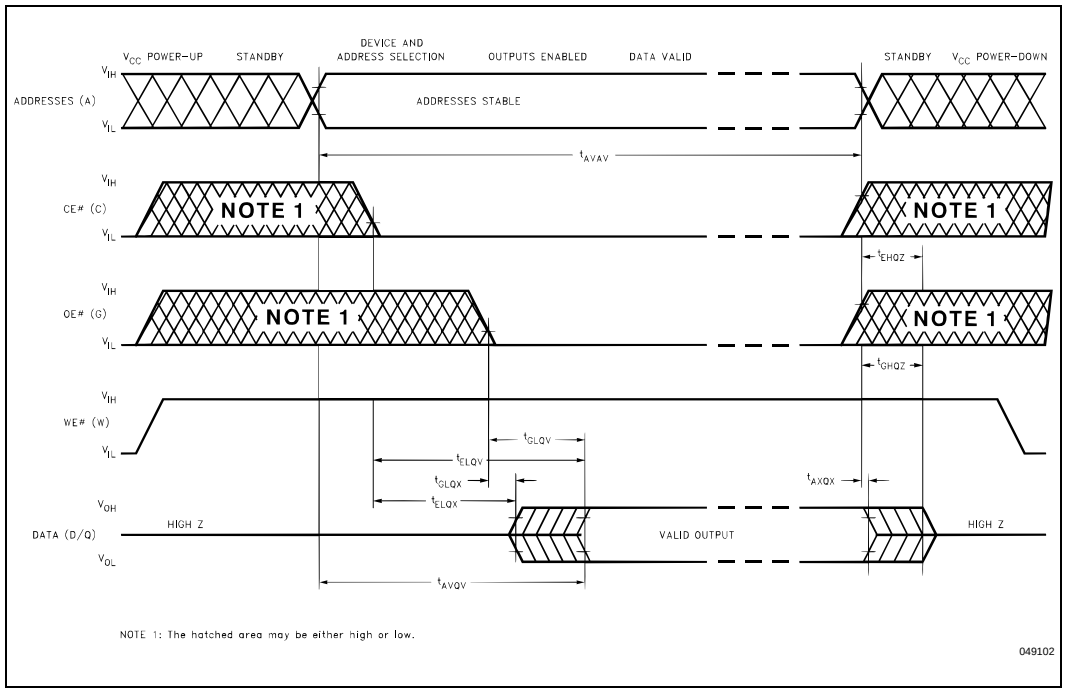


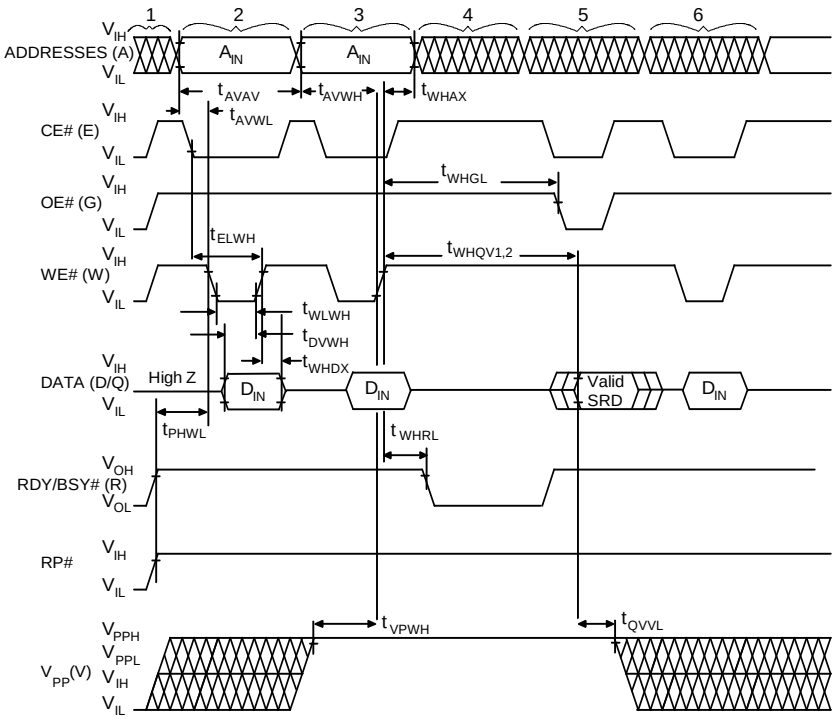
Figure 2. AC Waveforms for Read Operations

10.2 Write Operations: Common Memory(1)

Symbol		Parameter	100 ns at 5V		Unit
JEDEC	PCMCIA		Min	Max	
t_{AVAV}	t_cW	Write Cycle Time	100		ns
t_{WLWH}	t_w (WE)	Write Pulse Width	60		ns
t_{AVWL}	t_{su} (A)	Address Setup Time	10		ns
t_{AVWH}	t_{su} (A-WEH)	Address Setup Time for WE#	70		ns
t_{VPWH}	t_{vps}	V_{PP} Setup to WE# Going High	70		ns
t_{ELWH}	t_{su} (CEWEH)	Card Enable Setup Time for WE#	70		ns
t_{DVWH}	t_{su} (D-WEH)	Data Setup Time for WE#	40		ns
t_{WHDX}	t_h (D)	Data Hold Time	15		ns
t_{WHAX}	t_{rec} (WE)	Write Recovery Time	15		ns
t_{WHRL}		WE# High to RDY/BSY#			ns
t_{QVVL}		V_{PP} Hold from Operation Complete	0		ns
t_{WHGL}	t_h (OE-WE)	Output Enable Hold from WE#	10		ns
t_{PHWL}		Power-Down Recovery to WE# Going Low		1	µs

NOTE:

1. Read timing characteristics during erase and data program operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.



NOTES:

1. V_{CC} Power-Up and Standby
2. Write Program or Erase Setup Command
3. Write Valid Address and Program or Erase Confirm Command
4. Automated Program or Erase Delay
5. Read Status Register Data
6. Write Read Array Command

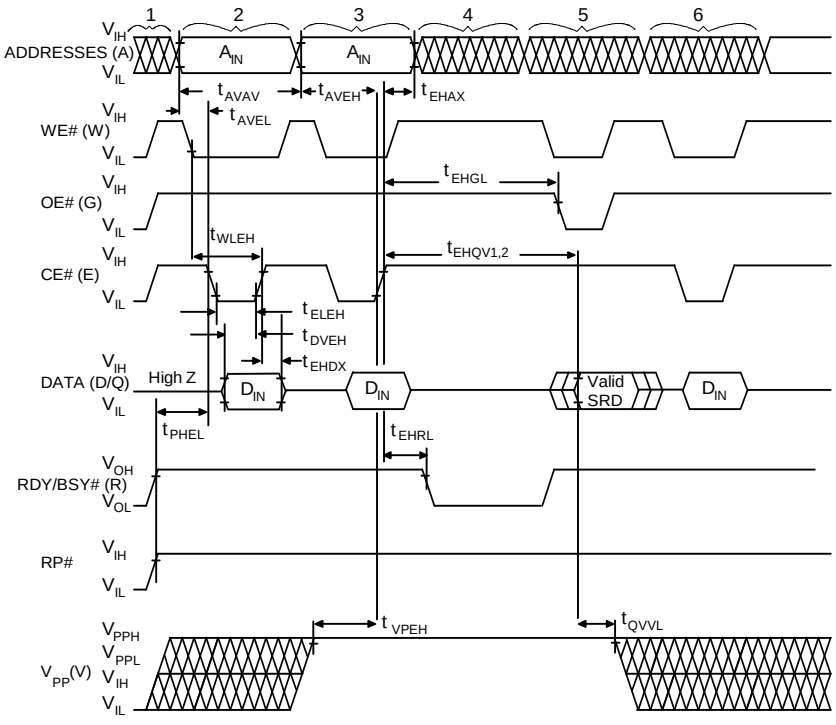
Figure 3. AC Waveforms for Write Operations

10.3 CE#-Controlled Write Operations: Common and Attribute Memory

Symbol		Parameter	100 ns at 5V		Unit
JEDEC	PCMCIA		Min	Max	
t_{AVAV}	t_cW	Write Cycle Time	100		ns
t_{ELEH}	t_w (WE)	Chip Enable Pulse Width	60		ns
t_{AVEL}	t_{su} (A)	Address Setup Time	10		ns
t_{AVEH}	t_{su} (A-WEH)	Address Setup Time for CE#	70		ns
t_{VPEH}	t_{vps}	V_{PP} Setup to CE# Going High	70		ns
t_{WLEH}	t_{su}(CE-WEH)	Write Enable Setup Time for CE#	70		ns
t_{DVEH}	t_{su} (D-WEH)	Data Setup Time for CE#	40		ns
t_{EHDX}	t_h (D)	Data Hold Time	15		ns
t_{EHAX}	t_{rec} (WE)	Write Recovery Time	15		ns
t_{EHRL}		CE# High to RDY/BSY#			ns
t_{QVVL}		V_{PP} Hold from Operation Complete	0		ns
t_{EHGL}	t_h (OE-WE)	Output Enable Hold from WE#	10		ns
t_{PHEL}		Power-Down Recovery to CE# Going Low		1	µs

NOTE:

1. Read timing characteristics during erase and program operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.



NOTES:

1. V_{CC} Power-Up and Standby
2. Write Program or Erase Setup Command
3. Write Valid Address and Program or Erase Confirm Command
4. AutomatedProgram or Erase Delay
5. Read Status Register Data
6. Write Read Array Command

Figure 4. Alternate AC Waveform for Write Operations

10.4 Power-Up/Power-Down

Symbol	Parameter	Notes	Min	Max	Units
PCMCIA					
V_i (CE)	CE# Signal Level (0.0V < V_{CC} < 2.0V)	1	0	V_{iMAX}	V
	CE# Signal Level (2.0V < V_{CC} < V_{IH})	1	V_{CC} – 0.1	V_{iMAX}	V
	CE# Signal Level (V_{IH} < V_{CC})	1	V_{IH}	V_{iMAX}	V
t_{su} (V_{CC})	CE# Setup Time		20		ms
t_{su} (RESET)	CE# Setup Time		20		ms
t_{rec} (V_{CC})	CE# Recover Time		1.0		µs
t_{pr}	V_{CC} Rising Time	2	0.1	300	ms
t_{pf}	V_{CC} Falling Time	2	3.0	300	ms
t_w (RESET)	RESET Width		10		µs
t_h (Hi-Z RESET)	RESET Width		1		ms
t_s (Hi-Z RESET)	RESET Width		0		ms

NOTES:

1. V_{iMAX} means Absolute Maximum Voltage for input in the period of 0.0V < V_{CC} < 2.0V, V_i (CE#) is only 0.00V ~ V_{iMAX}.
2. The t_{pr} and t_{pf} are defined as “linear waveforms” in the period of 10% to 90%, or vice-versa. Even if the waveform is not a “linear waveform,” its rising and falling time must meet this specification.

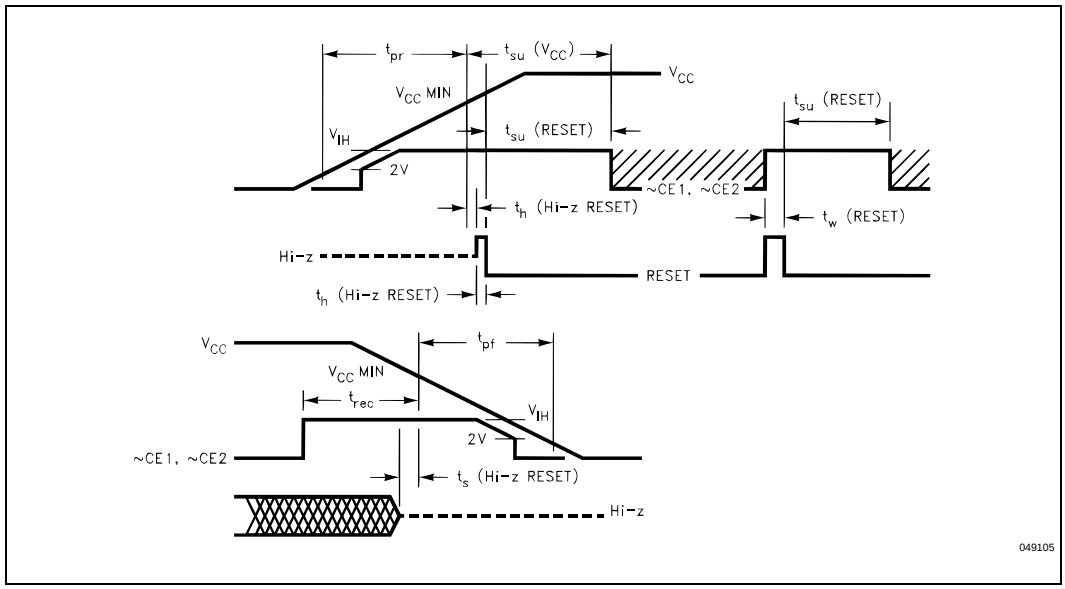


Figure 5. Power-Up/Down Timing for Systems Supporting RESET

11.0 CAPACITANCE

T_A = +25°C, f = 1.0 MHz

Symbol	Pins	Typ	Max	Unit
C_{IN}	Address/Control	25	50	pF
C_{IN}	V_{CC}	3	5	µF
C_{OUT}	Output	25	50	pF

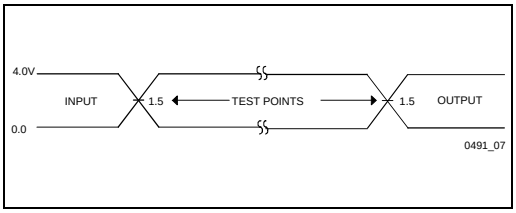


Figure 6. Transient Input/Output Reference Waveform for Standard Test Configuration

12.0 ERASE AND DATA WRITE PERFORMANCE(1,3)

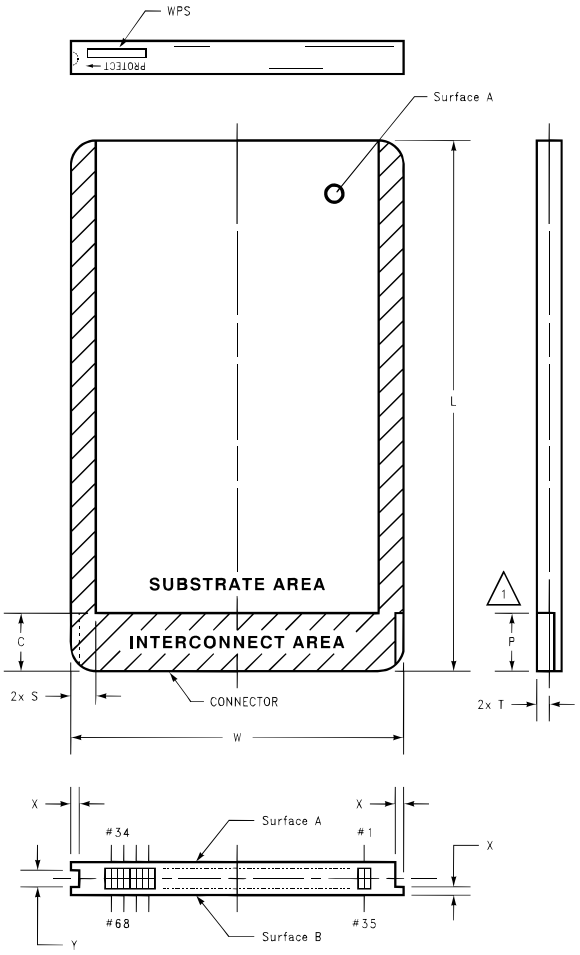
V_{CC} = 5V ± 0.5V, T_A = 0°C to +70°C

Sym	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
t_{WHOV1} t_{EHQV1}	Word/Byte Program Time	2,4		8 µs	3 ms		
t_{WHOV2} t_{EHQV2}	Block Program Time	2		0.4	2.1	sec	Word Program Mode
	Block Erase Time	2		0.6	10	sec	
	Full Chip Erase Time	2		38.4		sec	

NOTES:

1. +25°C, and normal voltages.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. To maximize system performance, the RDY/BSY# signal should be polled instead of using the maximum byte/word program time as a delay timer.
   The maximum word/byte program time is the absolute maximum time it takes the write algorithm to complete. The overwhelming majority of the bits program in the typical value specified.

13.0 PACKAGING



C MIN	L ± 0.008	P MIN △1	S MIN	T △2	W ± 0.004	X ± 0.002	Y ± 0.002
0.294 (†0.0)	3.370 (85.60)	0.394 (†0.0)	0.118 (3.0)	0.065 (1.65)	2.126 (54.0)	0.039 (1.00)	0.063 (1.60)

△1 POLARIZATION KEY LENGTH.

△2 INTERCONNECT AREA TOLERANCE = ±0.002
SUBSTRATE AREA TOLERANCE = ±0.004

3 MILLIMETERS ARE IN PARENTHESIS ().

049106

APPENDIX A
ORDERING INFORMATION

iMC008FLSC, SBXXXXX

Where:

i	= INTEL
MC	= MEMORY CARD
008	= DENSITY IN MEGABYTES (002, 004,008, 016 AVAILABLE)
FL	= FLASH TECHNOLOGY
S	= BLOCKED ARCHITECTURE
C	= REVISION
SBXXXXX	= CUSTOMER IDENTIFIER

APPENDIX B
ADDITIONAL INFORMATION

Order Number	Document
290429	*28F008SA 8-Mbit (1 Mbit x 8) FlashFile™ Memory Datasheet*
292158	*AP-606 Interchangeablility of Series 1, Series 2, and Series 2+ Flash Memory Cards*
292177	*AP-622 Value Series 100 Card Design*