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APPLICATION NOTE

Upgrade to the Value Series 100 Flash Memory Card

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TECHNICAL MARKETING
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INTRODUCTION

Removable linear memory storage offers several advantages over designing an on-board flash memory array:

- Density Upgrades
- Simple Code Updates
- PC Card Standard Pinout
- Multiple Card Vendors

Several features of the Series 2/2+ flash memory cards are unnecessary for embedded and PC applications. Customers often have to pay for additional flash card features they don't need, or could design around, in their system. The Value Series 100 flash memory card removes many of the unnecessary memory card features, it is simply a removable memory array of flash devices in a 68-Pin PC card form factor.

This document discusses how to reduce system cost and increase performance by designing with the Value Series 100 flash memory card. It also outlines simple software modifications for a system originally designed using Intel's Series 2/2+ flash memory cards. Software written for the Value Series 100 card will also work seamlessly with the Series 2/2+ cards.

NOTE:

The Intel Value Series 100 flash memory card has been designed to function in PCMCIA- compliant sockets without any hardware modifications. Simply update the system software for your next system shipment.

ARCHITECTURE

Earlier generation flash cards have ASICs to provide the Card Information Structure (CIS), Address/Data Path Logic, Attribute Memory Registers and Write Protection functionality. Intel's Value Series 100 flash memory card removes the ASICs and is basically an array of flash devices in a PC Card form factor, designed to offer the lowest cost code and data storage card solution with the added benefit of improved read performance and 5V operation.

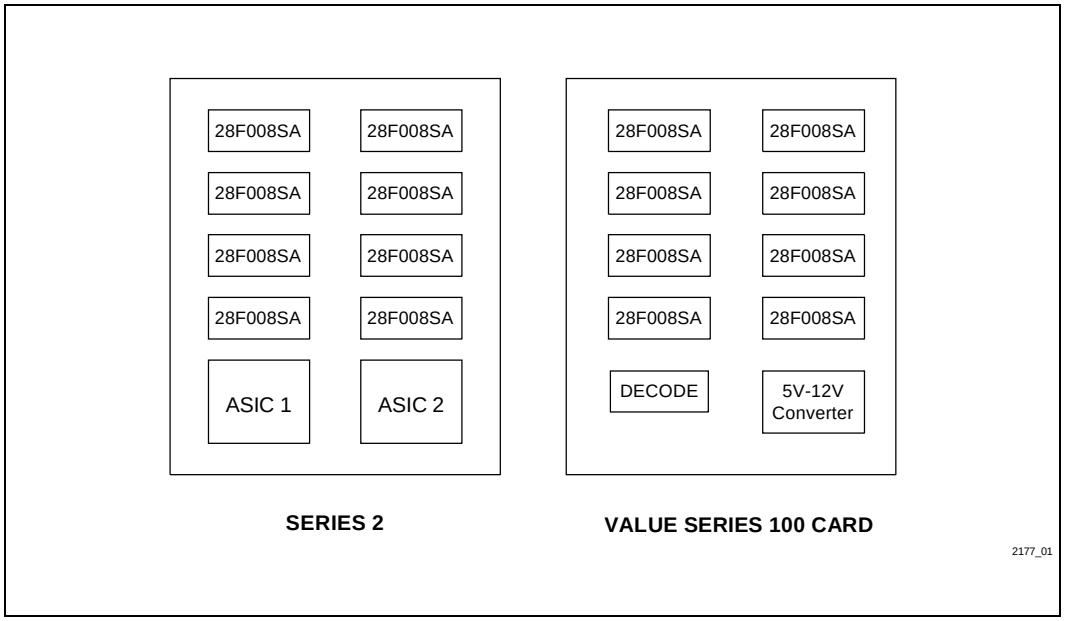

Figure 1. Flash Card Architecture

Value Series 100 Flash Memory Card Functionality: Quick Reference Guide

Section	Function	Value Series 100 Card	Series 2	Series 2+
	Component	**28F008SA**	**28F008SA**	**28F016SA**
1.0	Power Supply	5V Only	5V V_{CC} /12V V_{PP}	3.3V, 5.0V V_{CC} 3.3V, 5.0V, 12V V_{PP}
2.0	Software Algorithms	28F008SA Commands	28F008SA Commands	28F008SA and 28F016SA Enhanced Feature Commands
3.0	Card Recognition	CIS in Block 0 of Common Memory JEDEC ID: No CIS	CIS in Attribute Memory: REG# Functionality	CIS in Attribute Memory: REG# Functionality
4.0	Registers in Attribute Memory	No Attribute Memory ASIC Registers	ASIC Registers: – Soft Reset – Reset/Power-Down – Card Status – Write Protection – Sleep Control – Ready/Busy#	ASIC Registers: – Soft Reset – Reset/Power-Down – Card Status – Write Protection – Sleep Control – Ready/Busy# – Voltage Control
5.0	Address Decoding	Wraps at Card Density, A_0 is Not Decoded	A_0–A_{24} Decoded	A_0–A_{24} Decoded
6.0	Data Access	x16 Data Bus CE_1# => EVEN CE_2# => ODD	x8 or x16 Bus Width	x8 or x16 Bus Width
7.0	Write Protection	None.	WP Switch, Write Protection Register	WP Switch, Write Protection Register
8.0	Power-Down Mode	Reset/Power-Down Signal	Reset/ Power-Down Signal Reset/ Power-Down Register Sleep Control Register	Reset/ Power-Down Signal Reset/ Power-Down Register Sleep Control Register
9.0	RDY/BSY#	RDY/BSY# Signal Device Status Register	RDY/BSY# Signal Device Status Register Card Status Register Ready/Busy# Registers	RDY/BSY# Signal Device Status Register Card Status Registers Ready/Busy# Registers
10.0	Card Status	Device Status Register	Device Status Register Card Status Register	Device (Compatible) Status Register Card Status Register Block Status Register

1.0 POWER SUPPLY

The Value Series 100 flash memory card operates with a single 5.0V power supply. V_{CC} power is used during write and erase operations. **No external voltage converters are needed to supply the flash cards with 12V V_{PP}!** The V_{PP} lines on the Value Series 100 flash memory card are unconnected. 5V operation saves the system designer the converter cost and reduces the board space needed to support the Value Series 100 flash card.

2.0 SOFTWARE COMMANDS

The Value Series 100 flash memory card is based on the Intel 28F008SA flash component, the same components the Series 2 flash card utilizes, therefore, these cards share the same component software command set. The existing Read, Write and Erase commands and algorithms for a Series 2 card will work with the Value Series 100 card. The card status register is not available on the Value Series 100 flash memory card to detect the completion of a write or erase operation. The individual device status registers need to be checked for operation completion.

The Series 2+ Enhanced Performance Commands are not supported by the Value Series 100 flash memory card. These commands should not be used to access the components on the Value Series 100 flash memory card.

The Series 2/2+ flash cards have a Card Status Register (4100H in Attribute Memory) which is polled to determine the completion of a write/erase operation. The Value Series 100 flash memory card does NOT support the Card Status Register functionality. The completion of the write/erase operations can be verified by checking the individual Device Status Registers on the 28F008SA component.

NOTE:

Verify how software determines the completion of a write/erase algorithm for a Ready/Busy# Status. The software should read the individual Device Status Registers of the components on Value Series 100 flash memory card to determine when a write/erase operation has completed.

See Section 10.0 for more details.

3.0 CARD RECOGNITION

The Card Information Structure (CIS) is stored in the first Block 0 (128 KB) of Common Memory in the Even Byte memory locations. The Value Series 100 flash memory card does not implement a separate memory plane for the Attribute Memory Space. When system software attempts to read the CIS in attribute memory, the system will drive REG# low. REG# is unconnected on the Value Series 100 flash memory card side, and Common Memory containing the CIS tuples for the Value Series 100 flash memory card will be read instead. The Value Series 100 flash memory card tuple contains a Long Link Tuple that will point to Block Pair 1 in Common Memory (20000H) after the tuples have been parsed.

NOTE:

System software CANNOT use Block Pair 0 (Common Memory 00000H-1FFFFH) on the Value Series 100 flash memory card if the tuples are needed by the host system to identify the card. Many of the flash card formatters available will erase Block Pair 0 if the card is reformatted.

Tuple Reformatting

The tuples can be restored on a Value Series 100 flash memory card by downloading the CISer.EXE utility from the Intel BBS. Call the Intel BBS # at 1-800-356-3506.

No CIS Alternative

For some embedded and PC applications, the system might not need PCMCIA Tuples to determine the type of flash components and the card's density. The card can simply be accessed as an array of flash memory devices in a PCMCIA pinout. If tuples are not found on the card, the system can identify the components on the card by using the Read Intelligent Identifier Command (9090H). The Intelligent Identifier has a JEDEC manufacturer ID (8989H at Address 00H) and component ID (A2A2H at Address 02H) that can be used identify the density and block size of components on the card by using a software look-up table.

Determining Card Density without Using a CIS

After the components have been identified, the components need to be counted in order to determine the density of the flash array.

Put the first device pair in read ID mode by writing the Read Intelligent Identifier Command (9090H). Leave the components in read ID mode. After determining the size of the components on the memory card by using the lookup table, increment the address pointer to the next device pair boundary.

Attempt to read the component ID without putting the devices into the read ID mode. Successfully reading this device's ID indicates that the address generated a wrap-around condition and the system is back at the beginning of the memory array within the card.

If the component ID read was unsuccessful, put that device pair into read ID mode and perform a read to ensure a device pair is really present and increment the address pointer to the next component pair boundary.

Continue this process until every device pair in the card is accounted for, signaled by wrapping around and encountering the first device pair which was left in read ID mode or no device pair is present.

NOTE:

Remember to reset all device pairs to the read array mode after determining the card density.

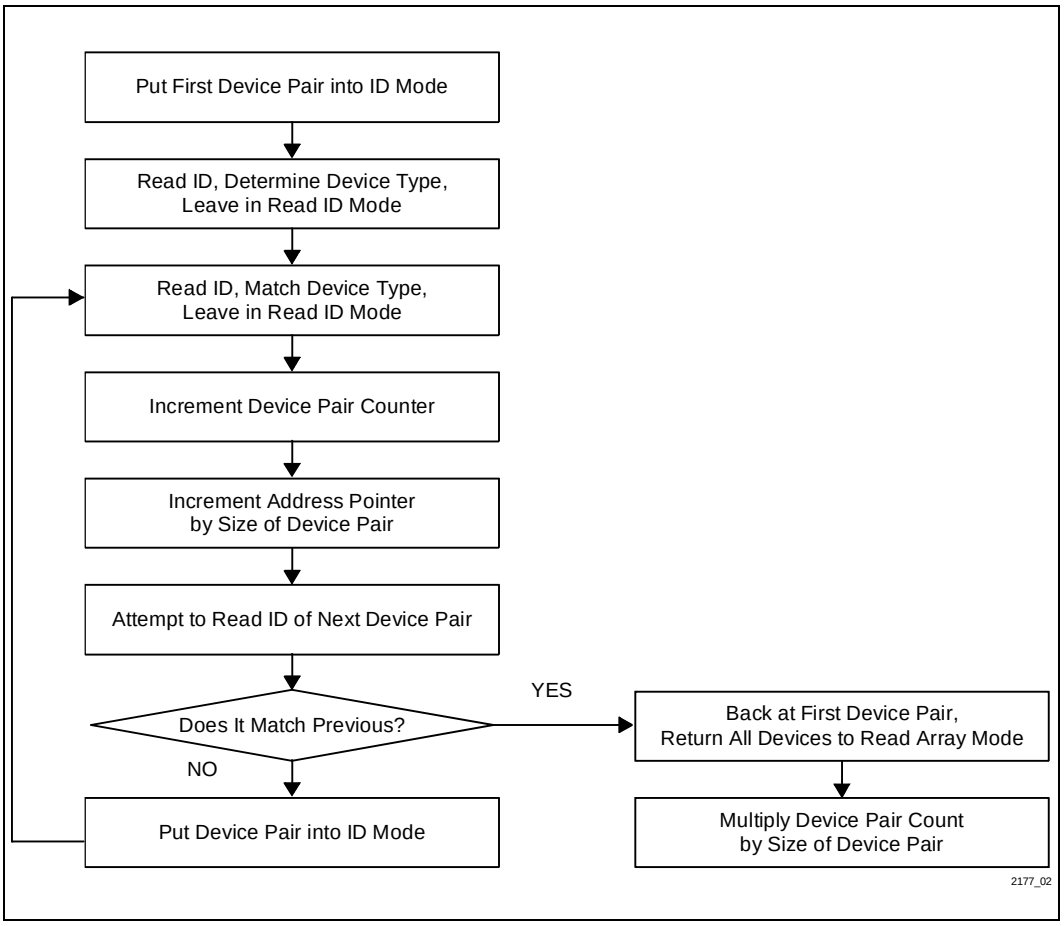

Figure 2. Card Density Determination

Table 1. Attribute Memory Register Implementations

Series 2/2+ Register	Attribute Address	Value Series 100 Flash Memory Card Alternative Functionality
Soft Reset Register	4000H	Assert the RESET signal to the card
Reset/Power-Down Register	4002H	Assert the RESET signal to the card
Sleep Control Register	4118H-411AH	Assert the RESET signal to the card
Card Status Register	4100H	Poll component Device Status Registers
Write Protection Register	4104H	No write protection; Switch V_{PP} to 0V
Ready/Busy Register	4120H-4140H	Poll component Device Status Registers
Voltage Control Register	410CH	No voltage control for the Value Series 100 flash memory card.

4.0 COMMAND REGISTERS

The Value Series 100 flash memory card does NOT have any of the Series 2/2+ Command Registers located in Attribute Memory (4000H-41FEH). Attempts to read or write the command registers in attribute memory by driving REG# LOW, will result in accesses to the Common Memory Plane on the Value Series 100 flash memory card. Software Writes to the Attribute Memory Registers does not change the data in flash memory.

The Command Register functionality on the Series 2/2+ flash memory card can still be realized on the Value Series 100 flash memory card by using PCMCIA signals on the card or the 28F008SA Device Status Registers. The functional alternatives listed in Table 1 would also be supported by the Series 2/2+ cards. The Value Series 100 flash memory card is a subset of the Series 2/2+ flash memory cards. Software written for the Values Series 100 flash memory card can support all three types of cards.

5.0 ADDRESS DECODING

The Value Series 100 flash memory card will wrap at the card's density, addresses lines beyond the density of the card will not be decoded. The system software should not try to write or read data to a memory area beyond the card's density.

The Series 2/2+ flash memory cards decode A_0-A_{25}, independent of the card density. The system designer should drive the unused upper address lines low to be backward compatible with the Series 2/2+ flash memory cards.

NOTE:

Verify that the system will not try to access memory beyond the card's density when upgrading to Value Series 100 flash memory cards. The host system should provide pull-down resistors or drive the upper address lines for Series 2/2+ compatibility

6.0 DATA ACCESS

The Value Series 100 flash memory card is a x16-only card, with individual byte control via CE_1# and CE_2#. EVEN bytes are always accessed on D_0–D_7 with CE_1# active, ODD bytes are always accessed on D_8–D_{15} with CE_2# active. The ODD bytes cannot be accessed on the lower data path D_0–D_7.

CAUTION:

This card will NOT function properly in x8 only systems that only use the lower data path, D_0–D_7.

The Series 2/2+ flash memory cards function in a x8/x16 mode, A_0 is decoded for any byte operation. To upgrade the system software for the Value Series 100 flash memory card, only x16-equivalent byte operations should be attempted by the software. Data accesses to the Value Series 100 flash memory card will work without any software modifications in systems that only execute word (x16) accesses.

Two methods for achieving x16-equivalent byte operations:

1. Odd byte operations: Shift byte operations to ODD addresses to the upper data path D_8–D_{15} and perform an odd byte operation with only CE_2# active, i.e., A_0 is ignored.
   Even byte operations: Normal Byte access using the lower data path D_0–D_7 with CE_1# active.
2. x16 write: When the system needs to do a byte write or read operation, perform a x16 write with FFH as the other data byte. Writing FFH to flash does NOT change the contents of the flash byte being written. For a x16 operation, A_0 will not be decoded.

7.0 WRITE PROTECTION

The Value Series 100 flash memory card does not have the ability to Write Protect areas of common memory, including the Card Information Structure stored in Block 0. The system software should NOT write/erase the Block 0 Flash area (00000H-1FFFFH) if the Block 0 PCMCIA Tuples are used for card identification.

8.0 POWER-DOWN MODE

The Value Series 100 flash memory card does NOT have the ability to power-down individual flash component pairs using the Sleep Control and Power-Down Registers located in attribute memory on the Series 2/2+ flash memory cards.

For reduced power consumption, the entire flash memory array can be powered-down for minimal current consumption by driving the RESET signal HIGH.

Since flash is a nonvolatile memory, power can be removed from the entire socket for ultimate power savings when the Value Series 100 flash memory card is not being accessed.

9.0 READY/BUSY# FUNCTIONALITY

The Ready/Busy# Status of the Value Series 100 flash memory card can be monitored two different ways via the Ready/Busy# signal or the Device Status Registers on the flash components.

The Ready/Busy# Signal ANDs the outputs of all the flash components and reports a BUSY Status if any component on the card is performing a write or erase operation. The system can wait until all the write/erase operations have completed before another operation can be attempted.

Another method to monitor the component status is by polling the individual Device Status Registers. Each component has a Device Status Register that reports the status of the Write State Machine. The component outputs Device Status Register information automatically after a Write(4040H) or Erase Command (2020H/D0D0H) has been issued. Another command cannot be issued to the Command User Interface until the Write State Machine becomes Ready.

One advantage polling the component Device Status Register has over the Ready/Busy# signal is that operations can be performed on other device pairs if one device pair is busy. The Device Status Register Polling technique will also work for the Series 2 and Series 2+ flash memory cards to simplify system software.

Example: An 8-MB card has four separate device pairs. If a block erase operation (2020H/D0D0H) gets issued to one of the device pairs, the three remaining component pairs are still Ready to accept operations, and can be accessed for read or write operations even though the Ready/Busy# Signal will report a BUSY status.

NOTE

Ready/Busy# mode (4140H in Attribute Memory), Ready/Busy# masking (4120H–4124H in Attribute Memory), and Ready/Busy# Status (4130H–4134H in Attribute Memory) functionality, which use the Attribute Memory Registers, is not supported by the Value Series 100 flash memory card. Software will need to be modified if the system uses the Series 2/2+ Registers in Attribute Memory for Ready/Busy# operation.

10.0 CARD STATUS

The Value Series 100 flash memory card does NOT have a Card Status Register (4100H in Attribute Memory) to report the overall card status. Much of the information reported in the Card Status Register for the Series 2/2+ flash memory cards does not apply to the Value Series 100 flash memory card.

The system software should read the individual component Device Status Registers by issuing the Read Status Register Command (7070H). The Device Status Register Information is automatically read after an Erase/Write command is issued.

The Device Status Register on the component returns the write state machine status, erase and erase suspend status, write status and Vpp status. When performing x16 write and erase operations, BOTH component Status Registers need to be checked for the completion and success of the operation.

Table 1. Device Status Register Definitions

WSMS	ESS	ES	BWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy

SR.6 = ERASE SUSPEND STATUS
1 = Erase Suspended
0 = Erase in Progress/Completed

SR.5 = ERASE STATUS
1 = Error in Block Erasure
0 = Successful Block Erase

SR.4 = BYTE WRITE STATUS
1 = Error in Byte Write
0 = Successful Byte Write

SR.3 = V_{PP} STATUS
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

SR.2-SR.0 = RESERVED FOR FUTURE ENHANCEMENTS

These bits are reserved for future use and should be masked out when polling the Status Register.

NOTES:

RY/BY# or the Write State Machine Status bit must first be checked to determine byte write or block erase completion, before the Byte Write or Erase Status bit are checked for success.

If the Byte Write *and* Erase Status bits are set to “1”s during a block erase attempt, an improper command sequence was entered. Attempt the operation again.

If V_{PP} low status is detected, the Status Register must be cleared before another byte write or block erase operation is attempted.

The V_{PP} Status bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates the V_{PP} level only after the Byte Write or Block Erase command sequence have been entered and informs the system if V_{PP} has not been switched on. The V_{PP} Status bit is not guaranteed to report accurate feedback between V_{PPL} and V_{PPH}.

ADDITIONAL INFORMATION

Revision History

Number	Description
-001	Original Version

Filename:	292177_1.DOC
Directory:	C:\TESTDOCS\DOCS
Template:	C:\WINDOWS\WINWORD6\TEMPLATE\ZAN____1.DOT
Title:	E
Subject:	
Author:	Mary Ann Hooker
Keywords:	
Comments:	
Creation Date:	08/26/95 9:01 AM
Revision Number:	29
Last Saved On:	12/06/95 10:05 AM
Last Saved By:	Ward McQueen
Total Editing Time:	253 Minutes
Last Printed On:	12/06/95 10:05 AM
As of Last Complete Printing	
Number of Pages:	9
Number of Words:	2,837 (approx.)
Number of Characters:	16,173 (approx.)