AP-606

APPLICATION NOTE

Interchangeability of Series 1, Series 2 and Series 2+ Flash Memory Cards

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1.0 INTRODUCTION

Many OEMs are incorporating PCMCIA-compatible card sockets into their computer systems. The benefits of using a removable memory media include easy system-to-system data transfer, rugged design, and easy density upgrades. However, this interchange capability presents the designer with the issue of ensuring system compatibility with the variety of available cards. As an example, OEMs wonder if their systems designed for the Series 2 or Series 2+ flash memory cards (or PCMCIA Release 2.1) will be compatible with Series 1 cards and vice versa.

NOTE

1. Series 2 cards refer to the iMC002FLSA, iMC004FLSA, iMC010FLSA, iMC020FLSA.
2. Series 2+ cards refer to the iMC004FLSP, iMC008FLSP, iMC020FLSP, iMC040FLSP.
3. Series 1 cards refer to the iMC001FLKA, iMC002FLKA, iMC004FLKA.

The purpose of this document is to discuss the ability of Series 1, Series 2 and Series 2+ flash memory cards to operate in systems designed using various PCMCIA releases. From a hardware standpoint, no modifications need to be made and software compatibility may be accomplished with minimal engineering effort. This document concentrates on the differences between the three types of Intel Flash cards, the flash memory devices within them, and how the cards operate with different PCMCIA Specification Releases.

2.0 INTEL FLASH MEMORY CARD FEATURES

To understand interchangeability, let's begin with a discussion of the Series 1, Series 2, and Series 2+ card features (refer to Table 1). All three cards contain ASICs that provide the PCMCIA-compatible electrical interface and decode and buffer circuitry for the flash memory devices. Only the Series 2 and Series 2+ cards have the additional benefits of a Card Information Structure (CIS) and Component Management Registers (CMRs). The CIS provides the system with pertinent information about the card, such as card density, manufacturer and device identification, access speed, etc. This information allows a software interpreter to easily determine the card type inserted into the system. The CMRs supply a software-controlled interface for the flash memory devices in the card.

2.1 Card Components

At the most fundamental level, the three card types utilize different types of flash memory devices; Series 1 cards contain ETOX™ II (28F010 and 28F020), Series 2 cards contain ETOX™ III (28F008SA) and Series 2+ cards contain ETOX™ IV (28F016SA) flash memory devices. The Series 1 card memory components are classified as bulk-erase flash memory. An erase operation erases each component in its entirety. The Series 2 and Series 2+ cards' memory components are FlashFile™ memory devices, separated into 64-Kbyte erasable blocks. These components have improved write and erase circuitry that perform the operations automatically after the system delivers the appropriate command. Write and erase completion can be determined by monitoring the cards RDY/BSY# output. (The detailed differences and examples of these write and erase operations will be discussed later in this document.) Additionally, the 28F008SA and 28F016SA components provide a deep power-down mode that greatly reduces power consumption in battery-powered systems.

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Table 1. Flash Card Feature Summary

	Series 1: iMCxxxFLKA	Series 2: iMCxxxFLSA	Series 2+: iMCxxxFLSP
Density (Megabytes)	1, 2, and 4	2, 4, 10, and 20	4, 8, 20 and 40
Flash Technology	ETOX II, 1.0 µ	ETOX III, 0.8 µ	ETOX IV, 0.6 µ
Erase Granularity	Bulk Erase: Full Chip	16–64-Kbyte Blocks Per Chip	32–64-Kbyte Blocks Per Chip
PCMCIA Compatibility	Release 1.0	Release 1.0, 2.0, 2.01 and 2.1	Release 1.0, 2.0, 2.01 and 2.1
Component Management Registers	No	Yes	Yes
Card Identification	Intelligent Identifier	Card Information Structure or Intelligent Identifier	Card Information Structure or Intelligent Identifier
Erase Operation	Requires SW or HW Timers	Automated (Uses RDY/BSY#)	Automated (Uses RDY/BSY#)
Erase Suspend	Not Applicable	Allows Read Priority	Allows Read/Write Priority
Data-Write Operation	Requires SW or HW Timers	Automated (Uses RDY/BSY#)	Automated (Uses RDY/BSY#)
Power-Down Mode	No	Yes	Yes
Power Supply Capabilities	5V V_{CC}/12V V_{PP}	5V V_{CC}/12V V_{PP}	3.3V ONLY or 5.0V ONLY or 3.3V_{CC}/12V_{PP} or 5.0V_{CC}/12V_{PP}
Individual Block Locks	No	No	Yes
Read Access Time	200 ns	200 ns	150 ns
Page Buffers	No	No	Yes

NOTE:
Highlighted areas show card generation improvements

3.0 HARDWARE CONSIDERATIONS

In this section we will examine the hardware differences between the PCMCIA Release 1.0 (R1.0) and Release 2.1 (R2.1) specifications. In particular, this section explains the results of plugging a Series 2 or Series 2+ card into a PCMCIA R1.0 socket and plugging a Series 1 card into a PCMCIA R2.1 socket.

3.1 Using a Series2/2+ Card in a PCMCIA R1.0 System

To be backwards-compatible, cards conforming to the PCMCIA R2.1 specification must function in a PCMCIA R1.0 socket. Four pin definitions were changed between PCMCIA R1.0 and R2.1. The Series 2/2+ card hardware has been designed to handle compatibility issues when plugging into a PCMCIA R1.0 socket.

3.1.1 RDY/BSY# PIN 16

Series 2 and Series 2+ cards output a RDY/BSY# (Pin 16) signal to monitor the status of the automated Write or Erase algorithm. Pin 16 on a PCMCIA R1.0 socket is a No Connect on the host side, incapable of RDY/BSY# functionality. Timing delays need to be implemented in software to allow the automated Write and Erase algorithms to successfully complete, since polling of the RDY/BSY# signal cannot be accomplished.

3.1.2 RESET: PIN 58

The PCMCIA R2.1 specification states that "Cards requiring RESET [such as the Series 2/2+ cards] must enter the unconfigured state each time power is applied." The RESET signal was not supported in a PCMCIA R1.0 system. To meet this requirement, the Series 2 and Series 2+ cards contain special circuitry to internally generate a power-on reset in less than one millisecond after power is applied. This functionality ensures that a card is reset when inserted into a PCMCIA R1.0-compatible socket. Note that all new socket designs must support the RESET signal to be PCMCIA R2.1 compatible.

CAUTION

A system designer may have tied PCMCIA R1.0 "No Connect Pins" to either V_{CC} or ground so the system outputs didn't float. Pin 58 tied to V_{CC} will cause a Series 2 or Series 2+ card to be in a constant state of RESET.

3.1.3 WAIT#: PIN 59

The WAIT# signal is asserted by a card to delay completion of the memory-access cycle in progress. The Series 2 and Series 2+ cards do not require this functionality; connecting the WAIT# signal to a "No-Connect" on a PCMCIA R1.0 host socket poses no problem. For PCMCIA R2.1 systems, the Series 2 and Series 2+ cards drive the WAIT# signal high to indicate an "always-accessible" status.

3.1.4 REG#: PIN 61

The REG# signal functionality was optional for PCMCIA R1.0 socket designs and a requirement for PCMCIA R2.0 and beyond. The Component Management Registers and Card Information Structure in the attribute memory plane of the Series 2 and Series 2+ flash memory cards cannot be accessed without REG# functionality.

What functionality do Series 2 and Series 2+ cards lose with the absence of REG# in a PCMCIA R1.0 socket?

Without REG#, a Series 2 CANNOT use:

- Software Reset Register
- Global Reset Power-Down Register
- Software Write Protection Register
- Software Sleep Control Register
- High-performance ready/busy mode
- Tuple information in the CIS

Without REG#, a Series 2+ card CANNOT:

- Use all Series 2 functionality listed above
- Operate in 3.3V or 5.0V only mode
- Erase locked blocks

Most of the performance features and design improvements the Series 2 and Series 2+ card offer CANNOT be fully realized in a PCMCIA R1.0 socket without REG# functionality. However, some customers may still opt to use a Series 2/2+ generation card in a PCMCIA R1.0 socket to obtain higher card densities or improved performance.

CAUTION

Memory blocks will be locked on a Series 2+ card as a safety precaution if power is interrupted (i.e., card is removed from the socket) during a Write or Erase command. The locked blocks cannot be unlocked in a system that does not support REG# functionality. A card partition with locked blocks cannot be reformatted.

3.1.5 ADDRESS LINES

The inputs to the address line on a PCMCIA R1.0-compliant socket should not cause any problems unless. . .

CAUTION

The upper address lines of a Series 1 card are "No Connects" on the card side. The upper address lines to the card socket may have been left floating and should not affect memory accesses to the card. The decoding circuitry on the Series 2 and Series 2+ decodes A_0–A_{25}. The upper address lines MUST be driven for the Series 2 and Series 2+ cards to prevent accesses to the wrong memory location.

3.2 Using a Series 1 Card in a PCMCIA R2.1 System

A system designed to meet PCMCIA R2.1 specifications supports the following signals which are not used on the Series 1 card: RDY/BSY#, RESET, REG# and WAIT#.

3.2.1 RDY/BSY#: PIN 16

The flash memory devices inside a Series 1 card do not have automated data-write and block-erase features and, therefore, do not support a RDY/BSY# interface. A card that supports the RDY/BSY# signal drives this signal high when the card is ready to be accessed. As specified by the PCMCIA R2.1 specification, the host system must provide a pull-up resistor (50 pF, 400 µA sink, 100 µA source) on this pin to accommodate Series 1 cards that do not support the RDY/BSY# signal. For a Series 1 card, system software must implement manual programming algorithms with timing delays to handle write and erase functionality (see Software Section 4.3).

3.2.2 RESET: PIN 58

The RESET signal, Pin 58, is input to a "No Connect" on the Series 1 card. The RESET signal is used by some PCMCIA cards to reset any internal registers or devices to an unconfigured state. Series 1 cards do not have any internal registers to reset and do not require RESET pin functionality. After starting a data-write or device-erase on a Series 1 card, the host may wish to abort the operation and reset the card. The abort operation can be done in software by issuing the Reset Command (FFH) directly to the Series 1 card devices.

3.2.3 WAIT#: PIN 59

The Series 1, Series 2 and Series 2+ cards do NOT support a WAIT-pin function. When used by other types of PC cards (such as modems or faxes), the WAIT# signal is asserted by a card to delay completion of the memory-access. To accommodate cards that do not support this signal, PCMCIA R2.1 and beyond requires a pull-up on the host system's interface (50 pF, 400 µA sink, 100 µA source).

3.2.4 REG#: PIN 61

The Series 1 flash memory card does not implement a PCMCIA Card Information Structure (CIS) in attribute memory, therefore eliminating the need to support a REG# pin. A Series 1 card can be formatted with a CIS located within the memory space taken from the bottom of available Common Memory to be PCMCIA R2.01-compliant. For the simple memory array contained within the card, practically all important details of the card can be determined by using the device ID mode and a lookup table stored within the code accessing the card. (Refer to Card Type Determination section.).

3.2.5 ADDRESS LINES

The upper address lines of a PCMCIA R2.1 socket will drive "No Connects" on Series 1 cards. To prevent memory wrap-around when trying to read from a Series 1 card, the system software should not attempt to access memory beyond the card's known capacity. See Section 4.1 and 4.2 to determine the component type and density for a Series 1 card.

3.3 Series 2+: Pin 43 VS1

PCMCIA redefined Pin 43 and Pin 57 as Voltage Sense Signals (Card Outputs) to detect whether or not a card is capable of operating in a 3.3V system. PCMCIA R1.0, R2.0, and R2.1 originally defined Pin 43 as a REFRESH signal for use with PSRAM cards. Series 2+ flash memory cards, which are capable of 3.3V operation, tie Pin 43 to GND to conform with the latest PCMCIA specification. VS2, Pin 57, was unused in previous PCMCIA revisions and remains unconnected for the Series 2+ card.

CAUTION

In systems which implemented the REFRESH functionality for PSRAM cards, the Series 2+ card VS1 signal tied to GND could cause the system to lock. The REFRESH functionality may need to be disabled on the older system for use with a Series 2+ card.

4.0 SOFTWARE DESIGN CONSIDERATIONS

This section will take a look at the various software-controlled functions involving Series 1, Series 2 and Series 2+ cards. It will describe how to determine the card type and size then subsequently choose the correct software algorithms to employ for writing and erasing data (aside from differing card densities and access speeds, all three cards are virtually identical from a read standpoint).

4.1 Card Determination

Using the Card Information Structure (CIS), the PCMCIA specification provides a standardized method for determining a card's characteristics in a PCMCIA R2.0 and beyond socket. Although a factory-ready, built-in CIS is not required, many cards include a CIS and therefore new systems should include software to interpret the CIS.

4.1.1 PCMCIA R1.0: NO REG# FUNCTIONALITY?

Some PCMCIA R1.0 sockets may have been designed without REG# functionality since the Series 1 card does NOT have an attribute memory plane. Software can identify the card type by issuing an Intelligent Identifier Command (9090H) and then reading the Manufacturing and Device codes. A look-up table can be referenced to identify the card type (see Table 2).

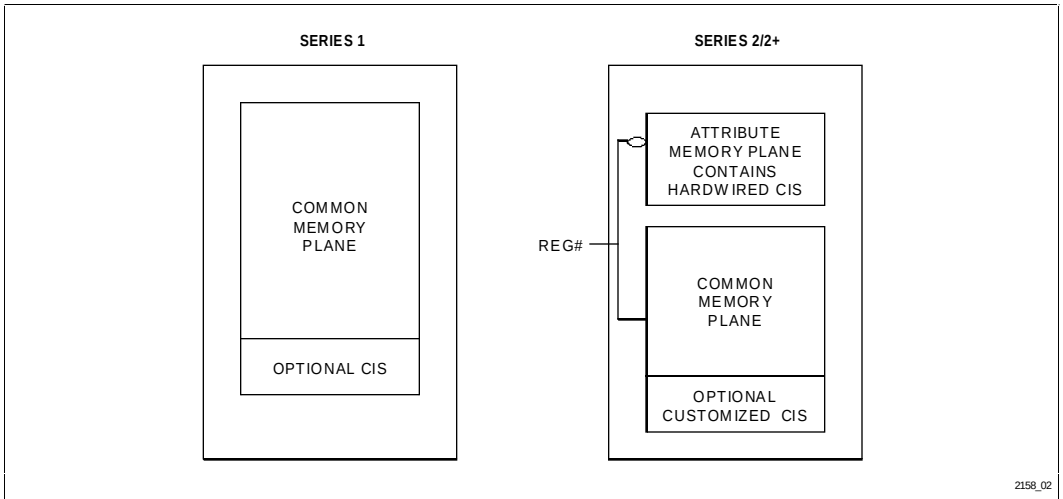
4.1.2 CARD INFORMATION STRUCTURE (CIS)

After inserting a memory card, the interpreter software should try to read the card's CIS. Using the word try indicates the possibility of finding a card without a CIS. To verify the presence of a CIS, the interpreter reads from the beginning of the CIS (Address 0000H of the Attribute Memory Plane, typically with REG# asserted) and determines a valid tuple (refer to PCMCIA spec). PCMCIA R2.1 specifies a minimal tuple requirement to meet the specification.

For example, with a Series 2 card, the CIS begins with a 01H, indicating the possibility of a Device Information Tuple. Further processing is done to determine if that Device Information Tuple really exists or that 01H signifies random data. The Device Information will contain information about the card's speed, type and size.

According to PCMCIA, a CIS can reside in two places within a memory card (see Figure 1):

1. In the Attribute Memory Plane, accessible using the REG# pin. The Series 2 and Series 2+ cards use the attribute memory plane implementation. The CIS contains card specific information: type of card, density, access speed, etc.
2. At the beginning of Common Memory, placed there by special format utilities provided by a system OEM or software vendor. Since a Series 1 card does not have an Attribute Memory Plane, this method can be used for Series 1 or PCMCIA R1.0 socket implementation, but is not required.



NOTES:
Optional CIS may be added by OEMs to customize Series 2/2+
A CIS can be written into the Common Memory Plane for Series 1 cards for PCMCIA R2.1 compatibility

Figure 1. Memory Structure of Flash Memory Cards

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4.2 Density Identification without a CIS

How does a system determine the card density, block count and size, etc. without using a CIS for the Series 1 card or in a PCMCIA R1.0 socket without REG# functionality? A "device ID lookup table" must be embedded in the card interpreter software. The software reads the first device pair's intelligent identifier (see Table 2), matches this value with one in the lookup table and increments the device pair counter (the card contains at least one device pair). Note that the first device pair is left in the read ID mode (see Figure 2).

After determining the component's size on the memory card by using the lookup table, increment the address pointer to the next device pair. Attempt to read the card ID without first putting it into the read ID mode. Successfully reading this device's ID indicates that the address generated a wrap-around condition and the system is back at the beginning of the memory array within the card. If the read was unsuccessful, put that device pair into read ID mode and perform a read to ensure a device pair is really present and increment the device-pair counter. Continue this process until every device pair in the card is accounted for, signaled by wrapping around and encountering the first device pair which was left in read ID mode or no device pair is present. **Remember to reset all device pairs to the read array mode after determining the card density.**

Table 2. Intelligent Identifier and Block Structure

Card Type	Intelligent Identifier		Component Type	Device Count	Number of Block Pairs	Block Pair Size
	0000H	0002H				
Series 1						
1 Meg	89H	B4H	28F010	8	4	128-Kwords
2 Meg	89H	BDH	28F020	8	4	256- Kwords
4 Meg	89H	BDH	28F020	16	8	256-Kwords
Series 2						
2 Meg	89H	A2H	28F008SA	2	16	64-Kwords
4 Meg	89H	A2H	28F008SA	4	32	64-Kwords
10 Meg	89H	A2H	28F008SA	10	80	64-Kwords
20 Meg	89H	A2H	28F008SA	20	160	64- Kwords
Series 2+						
4 Meg	89H	A0H	28F016SA	2	32	64-Kwords
8 Meg	89H	A0H	28F016SA	4	64	64-Kwords
20 Meg	89H	A0H	28F016SA	10	160	64-Kwords
40 Meg	89H	A0H	DD28F032SA	10	320	64-Kwords

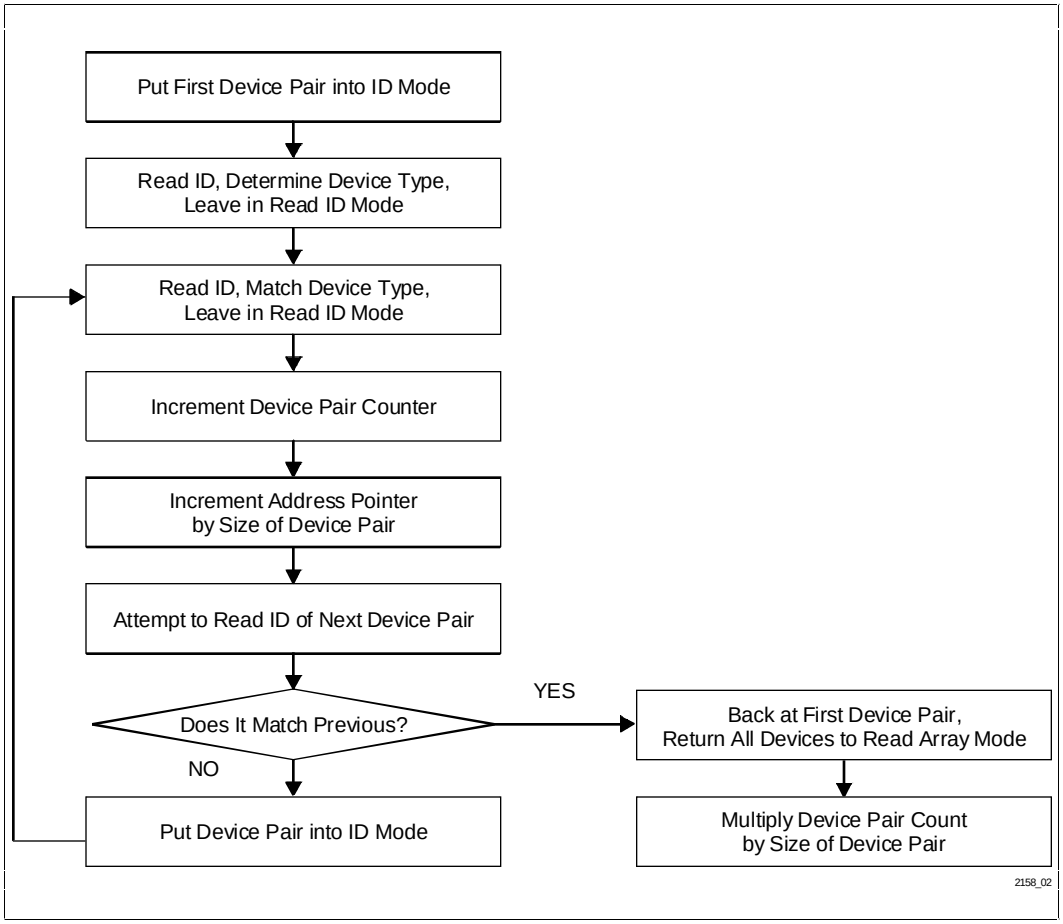

Figure 2. Card Density Determination

4.3 Write and Erase Algorithms

Similarities exist between Series 1, Series 2 and Series 2+ Write and Erase algorithms. For instance, to erase a device (or block), the system must first deliver an Erase Setup command followed by an Erase Confirm command. The biggest software differences exist in determining erase and write operation completion. Series 1 cards require the implementation of some sort of timer; either in software or hardware. The timer determines the length of the write or erase pulse. Series 2/2+ cards have automated Write/Erase algorithms.

4.3.1 PRE-CONDITIONING

Regardless of the card type, when erasing a flash device (or block), the region being erased must first be pre-conditioned by programming all bytes to zero before the actual erase operation begins. The flash devices in a Series 2 and Series 2+ card automatically perform this pre-conditioning as part of the overall erase process. Therefore, Series 2/2+ card software only needs to access a single byte location of the erase block to initiate an erase operation for the complete block.

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The software requirement is significantly different for a Series 1 card which requires manual pre-conditioning (and access to) of every byte within the erase region. This implies, that a system using a hardware paging scheme for addressing the memory of a Series 1 card (opposed to direct linear mapping), must switch pages (depending on the page size) to access the entire erase area.

4.3.2 WRITE/ERASE OPERATION COMPLETION

With Series 2 and Series 2+ cards, erase operations apply to blocks of a device rather than the entire device. (Refer to Figure 3 for an Erase algorithm comparison.) The completion of the operation can be determined by polling the RDY/BSY# signal output from the card. The Series 2 and Series 2+ cards automate the timer functions while writing or erasing, and can avoid system intervention until the system receives the ready signal from the card at the PCMCIA interface.

Series 1 cards require software or hardware timers to monitor the completion of a write or erase cycle. In a personal computer, the Erase algorithms of the Series 1 card can become a background task by taking advantage of the system timers in lieu of timing loops. The programmer can use either the system programmable timer through Interrupt 1CH or the time-of-day clock interrupt. Using the time-of-day clock interrupt, the system intervenes to perform an erase verify and initiate another erase pulse, every 55 milliseconds (the built-in stop timer of a Series 2/2+ device automatically cuts the erase pulse after 10 ms).

To demonstrate why a system designer might want to purposely decrease his system performance, assume an erase operation requires 50 pulses (10 ms each) to complete. Excluding system overhead, the erase operation would typically consume a total of 500 ms. In waiting for the 55 ms time-of-day clock, the flash device spends approximately 45 ms in an idle state in between erase pulses and the total erase operation increases to 2.75 seconds. In the ideal application this number becomes insignificant because that erase operation has occurred in the background, i.e., this erase area was “cleaning up” without impacting the user.

4.3.3 WRITE/ERASE VERIFICATION

The Series 1 memory card requires the software to perform an Erase/Write Verification after a Write/Erase command to ensure the operation has completed successfully. The Series 2/2+ memory cards have embedded the verification functionality into the Write/Erase algorithm. After a Write/Erase command has finished, a bit in the Device Status Register can be checked to see if the Write/Erase command completed successfully.

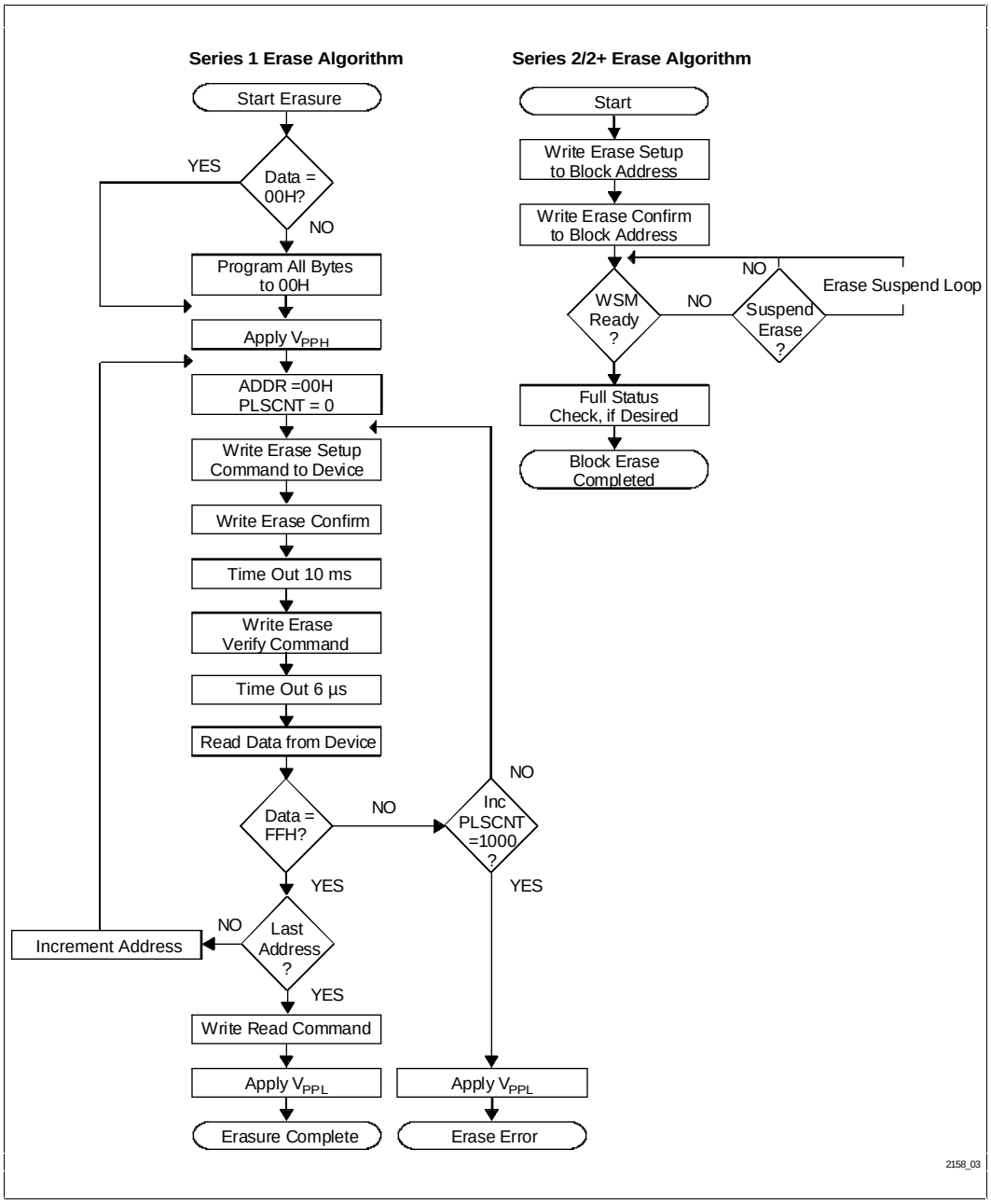

Figure 3. Series 1 versus Series 2/2+ Erase Algorithm Comparison

4.4 Command Comparison

Table 4 lists the differences in software commands used by the Series 1, Series 2 and Series 2+ flash memory cards.

4.5 Series 2 to Series 2+ Software Conversion

The Series 2+ flash memory card commands are a super-set to the existing Series 2 commands. A Series 2+ card is compatible with software written for a Series 2 card without any type of modification, given that the Series 2+ card can be recognized by the system.

The Series 2+ cards do have a set of "Performance Enhancement" commands (Table 3), in addition to the Series 2 compatible command set, which are used to exploit fully the enhanced feature set and performance improvement the Series 2+ card. For example: Series 2+ components have on-board page buffers which will improve the write speed to flash memory. Individual Block Locking, Page Buffer Writes, and RDY/BSY# modes are all controlled with the Series 2+ enhanced commands. Refer to the Series 2+ Flash Memory Card User's Manual (Order # 297373) for a detailed description of the features of the Series 2+ flash memory card.

Table 3. Series 2+ Performance Enhancement Commands

Code (H)	Series 2+ Command
08H	Page Buffer Write to Flash
71H	Read Extended Status Registers
72H	Page Buffer Swap
74H	Single Load to Page Buffer
75H	Read Page Buffer
77H	Lock Block
80H	Abort
96H	RDY/BSY# Reconfiguration
97H	Status Bits Upload
A7H	Erase All Unlocked Blocks
E0H	Sequential Load to Page Buffer
F0H	Sleep

Table 4. Software Command Comparison

	Series 1	Series 2	Series 2+ Compatible
Read Memory	00H	FFH	FFH
Intelligent ID Codes	90H	90H	90H
Set-up Erase/Erase Confirm	20H/20H	20H/D0H	20H/D0H
Erase Verify	A0H	Part of the Automated Erase Algorithm. Check Device Status Register	Part of the Automated Erase Algorithm. Check Device Status Register
Erase Suspend/Erase Resume	Issue Reset Command to Abort Erase Operation	B0H/D0H	B0H/D0H
Set-up Write/Write	40H	40H	40H
Alternate Write Set-Up/Write	No Alternate Write	10H	10H
Write Verify	C0H	Part of the Automated Write Algorithm. Check Device Status Register	Part of the Automated Write Algorithm. Check Device Status Register
Reset	FFH	FFH	FFH
Read Device Status Register	No Internal Registers	70H	70H
Clear Device Status Register	No Internal Registers	50H	50H

5.0 SUMMARY

This document shows that Series 1, Series 2 and Series 2+ cards have a high degree of interchangeability, given proper software and hardware design techniques. From a hardware standpoint, Series 1 cards plug into PCMCIA R2.1 systems and Series 2/2+ cards plug into PCMCIA R1.0 systems. Although exceptions do exist, it is strongly recommended that all new systems be designed to meet the requirements of the latest PCMCIA Version.

Software algorithm differences between the Series 1 and Series 2/2+ cards are different enough to require modifications, but a new system can easily have both algorithms embedded. The real difference is seen by the user, in the form of density options and a write performance perspective in disk emulation applications. The read performance difference will not be noticeable. However, because of higher densities, faster speeds and easier upgrade capabilities, Series 2/2+ cards should be phased-in as the long-term production vehicle for any system requiring high performance data storage from a nonvolatile PCMCIA R2.1 memory card.

Table 5. Common Problems and Troubleshooting Summary

	PCMCIA R1.0	PCMCIA R2.0
SERIES 1 iMCxxxFLKA	Does software support flash card?	Does software support flash card? No Attribute Memory Plane: No CIS No automated Write/Erase.
SERIES 2 iMCxxxFLSA	Does software support flash card? System Pin 58 (Card Reset) should be open or driven low. Is REG# (Pin 61) Functional? Upper address lines floating?	Does software support flash card?
SERIES 2+ iMCxxxFLSP	Does software support flash card? System Pin 58 (Card Reset) should be open or driven Low. Is REG# (Pin 61) functional? Upper address lines floating? Block-locking concerns?	Does software support flash card? V_{PP} generator turned ON in single voltage system?

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6.0 RELATED DOCUMENTS

Order Number	Document
290491	Series 2+ Flash Memory Cards 4-, 8-, 20- and 40-Megabyte Datasheet
290489	28F016SA 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory Datasheet
290434	Series 2 Flash Memory Cards iMC002FLSA, iMC004FLSA, iMC010FLSA, iMC020FLSA Datasheet
290429	28F008SA 8-Mbit (1-Mbit x 8) FlashFile™ Memory Datasheet
290388	iMC004FLKA 4-Mbyte Flash Memory Card Datasheet
290412	iMC002FLKA 2-Mbyte Flash Memory Card Datasheet
290399	iMC001FLKA 1-Mbyte Flash Memory Card Datasheet
290245	28F020 (256K x 8) 2048K CMOS Flash Memory Datasheet
290207	28F010 (128K x 8) 1024K CMOS Flash Memory Datasheet
292136	AB-56 “Preparing for the Next Generation Flash Memory Cards”
292095	AP-360 “28F008SA Software Drivers”
292096	AP-361 “Implementing the Integrated Registers of the Series 2 Flash Memory Card”
292099	AP-364 “28F008SA Automation and Algorithms”
292126	AP-377 “16-Mbit Flash Product Family Software Drivers”
292127	AP-378 “System Optimization Using the Enhanced Features of the 28F016SA”
297373	Series 2+ Flash Memory Card User’s Manual
297372	16-Mbit Flash Product Family User’s Manual
	PCMCIA 1.0 Specification
	PCMCIA 2.0 Specification
	PCMCIA 2.01 Specification
	PCMCIA 2.1 Specification