ADVANCE INFORMATION

A28F400BR-T/B
4-MBIT (256K X 16, 512K X 8)
SmartVoltage BOOT BLOCK FLASH MEMORY FAMILY

Automotive

- Intel SmartVoltage Technology
  - 5V or 12V Program/Erase
  - 5V Read Operation
- Very High Performance Read
  - 80 ns Max. Access Time
  - 40 ns Max. Output Enable Time
- Low Power Consumption
  - Maximum 60 mA Read Current at 5V
- x8/x16-Selectable Input/Output Bus
  - High Performance 16 or 32-bit CPUs
- Optimized Array Blocking Architecture
  - One 16-KB Protected Boot Block
  - Two 8-KB Parameter Blocks
  - One 96-KB Main Block
  - Three 128-KB Main Blocks
  - Top or Bottom Boot Locations
- Hardware-Protection for Boot Block
- Software EEPROM Emulation with Parameter Blocks
- Automotive Temperature Operation
  - −40°C to +125°C
- Extended Cycling Capability
  - 30,000 Block Erase Cycles for Parameter Blocks
  - 1,000 Block Erase Cycles for Main Blocks
- Automated Word/Byte Write and Block Erase
  - Industry-Standard Command User Interface
  - Status Registers
  - Erase Suspend Capability
- SRAM-Compatible Write Interface
- Automatic Power Savings Feature
  - 1 mA Typical I_{CC} Active Current in Static Operation
- Reset/Deep Power-Down Input
  - 0.2 μA I_{CC} Typical
  - Provides Reset for Boot Operations
- Hardware Data Protection Feature
  - Erase/Write Lockout during Power Transitions
- Industry-Standard Surface Mount Packaging
  - 44-Lead PSOP: JEDEC ROM Compatible
- ETOX™ IV Flash Technology

July 1996 Order Number: 290538-004

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect, IL 60056-7641

or call 1-800-879-4683

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CONTENTS PAGE

1.0 PRODUCT FAMILY OVERVIEW

This datasheet contains the specifications for the automotive version of the 28F400BR family of boot block flash memory devices.

This device continues to offer the same functionality as earlier BX devices but adds the capability of performing program and erase operations with a 5V or 12V V_{PP}. The A28F400BR automatically senses which voltage is applied to the V_{PP} pin and adjusts its operation accordingly.

1.1 New Features in the SmartVoltage Products

The new SmartVoltage boot block flash memory family offers identical operation as the current BX/BL 12V program products, except for the differences listed below. All other functions are equivalent to current products, including signatures, write commands, and pinouts.

- WP# pin has replaced a DU pin. See Table 1 for details.
- 5V Program/Erase operation has been added that uses proven program and erase techniques with 5V ± 10% applied to V_{PP}.

If you are designing with existing BX 12V V_{PP} boot block products today, you should provide the capability in your board design to upgrade to these new SmartVoltage products.

Follow these guidelines to ensure compatibilty:

1. Connect WP# (DU on existing products) to a control signal, V_{CC} or GND.
2. If adding a switch on V_{PP} for write protection, switch to GND for complete write protection.
3. Allow for connecting 5V to V_{PP} instead of 12V, if desired.

1.2 Main Features

Intel's SmartVoltage technology provides the most flexible voltage solution in the industry. SmartVoltage provides two discrete voltage supply pins, V_{CC} for read operation, and V_{PP} for Program and Erase operation. Discrete supply pins allow system designers to use the optimal voltage levels for their design. For program and erase operations, 5V V_{PP} operation eliminates the need for in system voltage converters, while 12V V_{PP} operation provides faster program and erase for situations where 12V is available, such as manufacturing or designs where 12V is already available.

The 28F400 boot block flash memory family is a very high-performance, 4-Mbit (4,194,304 bit) flash memory family organized as either 256 Kwords (262,144 words) of 16 bits each or 512 Kbytes (524,288 bytes) of 8 bits each.

Separately erasable blocks, including a hardware-lockable boot block (16,384 bytes), two parameter blocks (8,192 Bytes each) and main blocks (one block of 98,304 bytes and three blocks of 131,072 bytes), define the boot block flash family architecture. See Figure 3 for memory maps. Each parameter block can be independently erased and programmed 30,000 times. Each main or boot block can be erased 1,000 times.

The boot block is located at either the top (denoted by -T suffix) or the bottom (-B suffix) of the address map in order to accommodate different microprocessor protocols for boot code location. The hardware-lockable boot block provides complete code security for the kernel code required for system initialization. Locking and unlocking of the boot block is controlled by WP# and/or RP# (see Section 3.4 for details).

The Command User Interface (CUI) serves as the interface between the microprocessor or microcontroller and the internal operation of the boot block flash memory products. The internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for program and erase operations, including verifications, thereby unburdening the microprocessor or microcontroller of these tasks. The Status Register (SR) indicates the status of the WSM and whether it successfully completed the desired program or erase operation.

Program and Erase Automation allows program and Erase operations to be executed using an industry-standard two-write command sequence to the CUI. Data writes are performed in word or byte increments. Each byte or word in the flash memory can be programmed independently of other memory locations, unlike erases, which erase all locations within a block simultaneously.

The 4-Mbit SmartVoltage boot block flash memory family is also designed with an Automatic Power Savings (APS) feature which minimizes system battery current drain, allowing for very low power designs. To provide even greater power savings, the boot block family includes a deep power-down mode which minimizes power consumption by turning most of the Flash memory's circuitry off. This mode is controlled by the RP# pin and its usage is discussed in Section 3.5, along with other power consumption issues.

Additionally, the RP# pin provides protection against unwanted command writes due to invalid system bus conditions that may occur during system reset and power-up/down sequences. Also, when the Flash memory powers-up, it automatically defaults to the read array mode, but during a warm system reset, where power continues uninterrupted to the system components, the flash memory could remain in a non-read mode, such as erase. Consequently, the system Reset pin should be tied to RP# to reset the memory to normal read mode upon activation of the Reset pin.

The byte-wide or word-wide input/output is controlled by the BYTE# pin. See Table 1 for a detailed description of BYTE# operations, especially the usage of the DQ_{15}/A_{-1} pin.

The 28F400 products are available in a ROM/EPROM-compatible pinout and housed in the 44-lead PSOP (Plastic Small Outline) package.

Refer to the DC Characteristics Table Section 5.2 for complete current and voltage specifications. Refer to the AC Characteristics Table, Section 5.3, for read, write and erase performance specifications.

1.3 Applications

The 4-Mbit boot block flash memory family combines high-density, low-power, high-performance, cost-effective flash memories with blocking and hardware protection capabilities. Their flexibility and versatility reduce costs throughout the product life cycle. Flash memory is ideal for Just-In-Time production flow, reducing system inventory and costs, and eliminating component handling during the production phase.

When the product is in the end-user's hands, and updates or feature enhancements become necessary or mandatory, flash memory eliminates the need to replace an assembly. The update can be performed as part of routine maintenance operation by relatively unsophisticated technicians.

The reliability of such a field upgrade is enhanced by a hardware-protected 16-Kbyte boot block. If the protection methods are implemented in the circuit design, the boot block will be unchangeable. Locating the boot-strap code in this area assures a fail-safe recovery from an update operation that failed to complete correctly.

The two 8-Kbyte parameter blocks allow modification of control algorithms to reflect changes in the process or device being controlled. A variety of software algorithms allow these two blocks to behave like a standard EEPROM.

Intel's boot block architecture provides a flexible voltage solution for the different design needs of various applications. The asymmetrically blocked memory map allows the integration of several memory components into a single Flash device. The boot block provides a secure boot PROM; the parameter blocks can emulate EEPROM functionality for parameter store with proper software techniques; and the main blocks provide code and data storage with access times fast enough to execute code in place, decreasing RAM requirements.

1.4 Pinouts

Intel's SmartVoltage Boot Block architecture provides upgrade paths in every package pinout to the 8-Mbit density. The 28F400 44-lead PSOP pinout follows the industry standard ROM/EPROM pinout as shown in Figure 2.

Pinouts for the corresponding 2-Mbit and 8-Mbit components are also provided for convenient reference. 4-Mbit pinouts are given on the chip illustration in the center, with 2-Mbit and 8-Mbit pinouts going outward from the center.

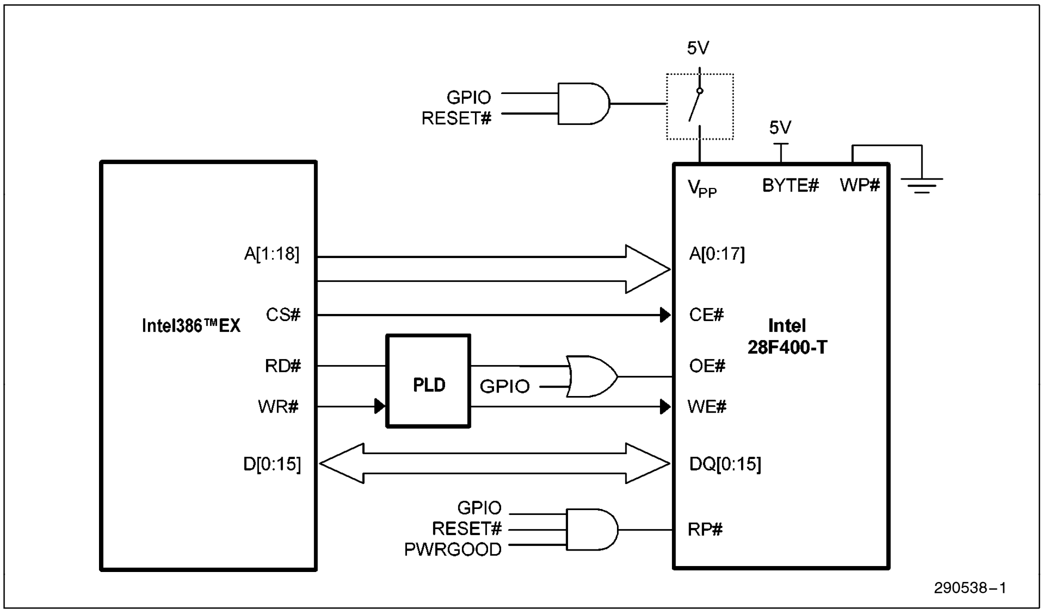
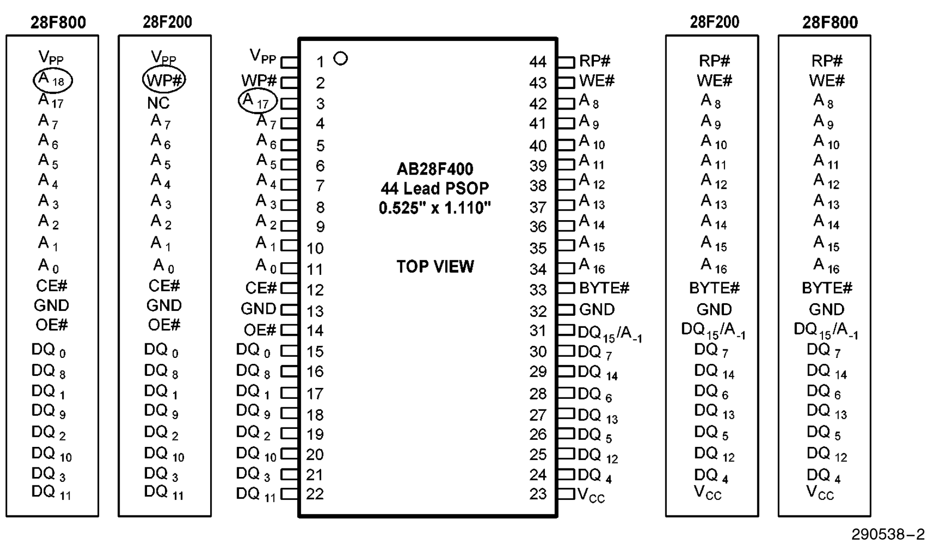


Figure 1. 28F400BX Interface to Intel386™ Microprocessor



NOTE:
Pin 2 is DU for BX 12V V_{PP} Versions.

Figure 2. 44-Lead PSOP Lead Configuration for x8/x16 28F400 Is Compatible with 2 and 8 Mbit.

1.5 Pin Descriptions

Table 1. 28F400 Pin Descriptions

Symbol	Type	Name and Function
A_0–A_{17}	INPUT	**ADDRESS INPUTS:** for memory addresses. Addresses are internally latched during a write cycle.
A_9	INPUT	**ADDRESS INPUT:** When A_9 is at V_{HH} the signature mode is accessed. During this mode, A_0 decodes between the manufacturer and device IDs. When BYTE# is at a logic low, only the lower byte of the signatures are read. DQ_{15}/A_{-1} is a don't care in the signature mode when BYTE# is low.
DQ_0–DQ_7	INPUT/OUTPUT	**DATA INPUTS/OUTPUTS:** Inputs array data on the second CE# and WE# cycle during a Program command. Inputs commands to the Command User Interface when CE# and WE# are active. Data is internally latched during the Write cycle. Outputs array, Intelligent Identifier and Status Register data. The data pins float to tri-state when the chip is de-selected or the outputs are disabled.
DQ_8–DQ_{15}	INPUT/OUTPUT	**DATA INPUTS/OUTPUTS:** Inputs array data on the second CE# and WE# cycle during a Program command. Data is internally latched during the Write cycle. Outputs array data. The data pins float to tri-state when the chip is de-selected or the outputs are disabled as in the byte-wide mode (BYTE# = "0"). In the byte-wide mode DQ_{15}/A_{-1} becomes the lowest order address for data output on DQ_0–DQ_7.
CE#	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. CE# is active low. CE# high de-selects the memory device and reduces power consumption to standby levels. If CE# and RP# are high, but not at a CMOS high level, the standby current will increase due to current flow through the CE# and RP# input stages.
OE#	INPUT	**OUTPUT ENABLE:** Enables the device's outputs through the data buffers during a read cycle. OE# is active low.
WE#	INPUT	**WRITE ENABLE:** Controls writes to the Command Register and array blocks. WE# is active low. Addresses and data are latched on the rising edge of the WE# pulse.
RP#	INPUT	**RESET/DEEP POWER-DOWN:** Uses three voltage levels (V_{IL}, V_{IH}, and V_{HH}) to control two different functions: reset/deep power-down mode and boot block unlocking. It is backwards-compatible with the 28F400BX/BL. **When RP# is at logic low, the device is in reset/deep power-down mode,** which puts the outputs at High-Z, resets the Write State Machine, and draws minimum current. **When RP# is at logic high, the device is in standard operation.** When RP# transitions from logic-low to logic-high, the device defaults to the read array mode. **When RP# is at V_{HH}, the boot block is unlocked** and can be programmed or erased. This overides any control from the WP# input.

Table 1. 28F400 Pin Descriptions (Continued)

Symbol	Type	Name and Function
WP#	INPUT	**WRITE PROTECT:** Provides a method for unlocking the boot block in a system without a 12V supply. **When WP# is at logic low, the boot block is locked,** preventing Program and Erase operations to the boot block. If a Program or Erase operation is attempted on the boot block when WP# is low, the corresponding status bit (bit 4 for Program, bit 5 for Erase) will be set in the Status Register to indicate the operation failed. **When WP# is at logic high, the boot block is unlocked** and can be programmed or erased. **NOTE:** This feature is overridden and the boot block unlocked when RP# is at V_{HH}. See Section 3.4 for details on write protection.
BYTE#	INPUT	**BYTE# ENABLE:** Controls whether the device operates in the byte-wide (x8) mode or the word (x16) mode. The BYTE# input must be controlled at CMOS levels to meet the CMOS current specification in the standby mode. When BYTE# is at logic low, the byte-wide mode is enabled. A 19 bit address is applied on A_{-1} to A_{17}, and 8 bits of data is read and written on DQ_0–DQ_7. When BYTE# is at logic high, the word-wide mode is enable. An 18 bit address is applied on A_0 to A_{17} and 16 bits of data is read and written on DQ_0–DQ_{15}.
V_{CC}		**DEVICE POWER SUPPLY:** 5.0V ± 10%
V_{PP}		**PROGRAM/ERASE POWER SUPPLY:** For erasing memory array blocks or programming data in each block, a voltage either of 5V ± 10% or 12V ± 5% must be applied to this pin. When $V_{PP} < V_{PPLK}$ all blocks are locked and protected against Program and Erase commands.
GND		**GROUND:** For all internal circuitry.
NC		**NO CONNECT:** Pin may be driven or left floating.

2.0 PRODUCT DESCRIPTON

2.1 Memory Organization

2.1.1 BLOCKING

This product family features an asymmetrically blocked architecture enhancing system memory integration. Each block can be erased independently. The block sizes have been chosen to optimize their functionality for common applications of nonvolatile storage. For the address locations of the blocks, see the memory maps in Figure 3.

2.1.1.1 Boot Block - 1 x 16 KB

The boot block is intended to replace a dedicated boot PROM in a microprocessor or microcontroller-based system. The 16-Kbyte (16,384 bytes) boot block is located at either the top (denoted by -T suffix) or the bottom (-B suffix) of the address map to accommodate different microprocessor protocols for boot code location. This boot block features hardware controllable write-protection to protect the crucial microprocessor boot code from accidental erasure. The protection of the boot block is controlled using a combination of the V_{PP}, RP#, and WP# pins, as is detailed in Table 8.

2.1.1.2 Parameter Blocks - 2 x 8 KB

The boot block architecture includes parameter blocks to facilitate storage of frequently updated small parameters that would normally require an EEPROM. By using software techniques, the byte-rewrite functionality of EEPROMs can be emulated. These techniques are detailed in Intel's AP-604, "Using Intel's Boot Block Flash Memory Parameter Blocks to Replace EEPROM." Each boot block component contains two parameter blocks of eight Kbytes (8,192 bytes) each. The parameter blocks are not write-protectable.

2.1.1.3 Main Blocks - 1 x 96 KB + 3 x 128 KB

After the allocation of address space to the boot and parameter blocks, the remainder is divided into main blocks for data or code storage. Each 4-Mbit device contains one 96-Kbyte (98,304 byte) block and three 128-Kbyte (131,072 byte) blocks. See the memory maps for each device for more information.

3.0 PRODUCT FAMILY PRINCIPLES OF OPERATION

Flash memory augments EPROM functionality with in-circuit electrical write and erase. The boot block flash family utilizes a Command User Interface (CUI) and automated algorithms to simplify write and erase operations. The CUI allows for 100% TTL-level control inputs, fixed power supplies during erasure and programming, and maximum EPROM compatibility.

When $V_{PP} < V_{PPLK}$, the device will only successfully execute the following commands: Read Array, Read Status Register, Clear Status Register and intelligent identifier mode. The device provides standard EPROM Read, Standby and Output Disable operations. Manufacturer Identification and Device Identification data can be accessed through the CUI or through the standard EPROM A_9 high voltage access (V_{ID}) for PROM programming equipment.

The same EPROM Read, Standby and Output Disable functions are available when 5V or 12V is applied to the V_{PP} pin. In addition, 5V or 12V on V_{PP} allows write and erase of the device. All functions associated with altering memory contents: Write and Erase, Intelligent Identifier Read, and Read Status are accessed via the CUI.

The purpose of the Write State Machine (WSM) is to completely automate the write and erasure of the device. The WSM will begin operation upon receipt of a signal from the CUI and will report status back through a Status Register. The CUI will handle the WE# interface to the data and address latches, as well as system software requests for status while the WSM is in operation.

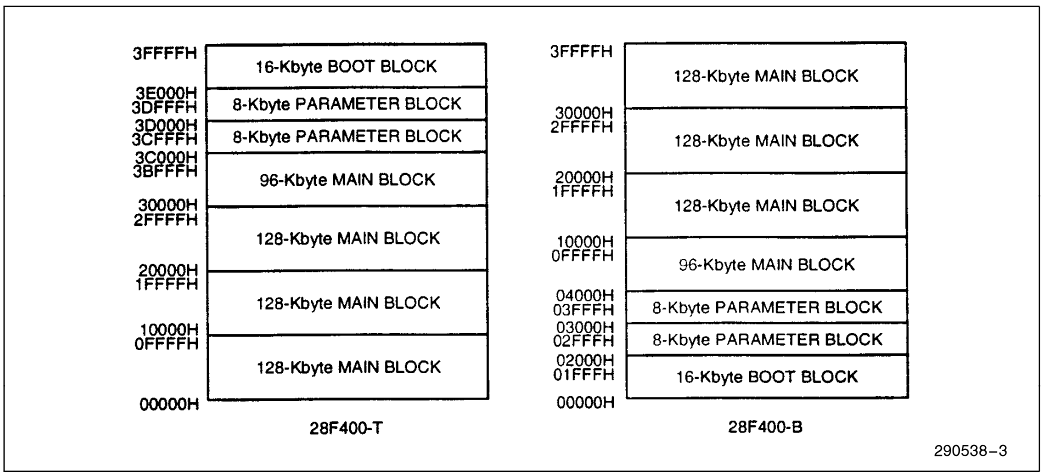


Figure 3. 28F400-T/B Memory Maps

Table 2. Bus Operations for Word-Wide Mode (BYTE# = V_{IH})

Mode	Notes	RP#	CE#	OE#	WE#	A_9	A_0	V_{PP}	DQ_{0-15}
Read	1,2,3	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	X	D_{OUT}
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	X	High Z
Standby		V_{IH}	V_{IH}	X	X	X	X	X	High Z
Deep Power-Down	9	V_{IL}	X	X	X	X	X	X	High Z
Intelligent Identifier (Mfr)	4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IL}	X	0089 H
Intelligent Identifier (Device)	4,5	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IH}	X	See Table 4
Write	6,7,8	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	X	D_{IN}

Table 3. Bus Operations for Byte-Wide Mode (BYTE# = V_{IL})

Mode	Notes	RP#	CE#	OE#	WE#	A_9	A_0	A_{-1}	V_{PP}	DQ_{0-7}	DQ_{8-14}
Read	1,2,3	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	X	X	D_{OUT}	High Z
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	X	X	High Z	High Z
Standby		V_{IH}	V_{IH}	X	X	X	X	X	X	High Z	High Z
Deep Power-Down	9	V_{IL}	X	X	X	X	X	X	X	High Z	High Z
Intelligent Identifier (Mfr)	4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IL}	X	X	89H	High Z
Intelligent Identifier (Device)	4,5	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IH}	X	X	See Table 4	High Z
Write	6,7,8	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	X	X	D_{IN}	High Z

NOTES:

1. Refer to DC Characteristics.
2. X can be V_{IL}, V_{IH} for control pins and addresses, V_{PPLK} or V_{PPH} for V_{PP}.
3. See DC Characteristics for V_{PPLK}, $V_{PPH}1$, $V_{PPH}2$, V_{HH}, V_{ID} voltages.
4. Manufacturer and Device codes may also be accessed via a CUI write sequence, A_1–A_{17} = X, A_1–A_{18} = X.
5. See Table 4 of Device IDs.
6. Refer to Table 5 for valid D_{IN} during a Write operation.
7. Command writes for Block Erase or Word/Byte Write are only executed when V_{PP} = $V_{PPH}1$ or $V_{PPH}2$.
8. To Write or Erase the boot block, hold RP# at V_{HH} or WP# at V_{IH}.
9. RP# must be at GND ± 0.2V to meet the maximum deep power-down current specified.

3.1 Bus Operations

Flash memory reads, erases and writes in-system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles. These bus operations are summarized in Tables 2 and 3.

3.2 Read Operations

The boot block flash device has three user read modes: array, intelligent identifier, and status register. Status register read mode will be discussed, in detail, in Section 3.3.2.

3.2.1 READ ARRAY

When RP# transitions from V_{IL} (reset) to V_{IH}, the device will be in the read array mode and will respond to the read control inputs (CE#, address inputs, and OE#) without any commands being written to the CUI.

When the device is in the read array mode, five control signals must be controlled to obtain data at the outputs.

- WE# must be logic high (V_{IH})
- CE# must be logic low (V_{IL})
- OE must be logic low (V_{IL})
- RP# must be logic high (V_{IH})
- BYTE# must be logic high or logic low.

In addition, the address of the desired location must be applied to the address pins. Refer to Figure 10 and 11 for the exact sequence and timing of these signals.

If the device is not in read array mode, as would be the case after a Program or Erase operation, the Read Mode command (FFH) must be written to the CUI before reads can take place.

3.2.1.1 Output Control

With OE# at logic-high level (V_{IH}), the output from the device is disabled and data Input/Output pins (DQ[0:15] or DQ[0:7]) are tri-stated.

3.2.1.2 Input Control

With WE# at logic-high level (V_{IH}), input to the device is disabled.

3.2.2 INTELLIGENT IDENTIFIERS

The intelligent identifiers of the SmartVoltage boot block components are identical to the boot block products that operate only at 12V V_{PP}. The manufacturer and device codes are read via the CUI or by taking the A_9 pin to V_{ID}. Writing 90H to the CUI places the device into intelligent identifier read mode. In this mode, $A_0 = 0$ outputs the manufacturer's identification code and $A_0 = 1$ outputs the device code. When BYTE# is at a logic low, only the lower byte of the above signatures is read and DQ_{15}/A_{-1} is a "don't care" during intelligent identifier mode. See the table below for product signatures. A Read Array command must be written to the memory to return to the read array mode.

Table 4. Intelligent Identifier Table

Product	Mfr. ID	Device ID	
		-T (Top Boot)	-B (Bottom Boot)
28F400	0089 H	4470 H	4471 H

3.3 Write Operations

3.3.1 COMMAND USER INTERFACE (CUI)

The Command User Interface (CUI) serves as the interface between the microprocessor and the internal chip controller. Commands are written to the CUI using standard microprocessor write timings. The available commands are Read Array, Read Intelligent Identifier, Read Status Register, Clear Status Register, Erase and Program (summarized in Tables 5 and 6). For Read commands, the CUI points the read path at either the array, the intelligent identifier, or the Status Register depending on the command received. For Program or Erase commands, the CUI informs the Write State Machine (WSM) that a write or erase has been requested. During the execution of a Program command, the WSM will control the programming sequences and the CUI will only respond to status reads. During an erase cycle, the CUI will respond to status reads and erase

Table 5. Command Set Codes and Corresponding Device Mode

Command Codes	Device Mode
00	Invalid Reserved
10	Alternate Program Set-Up
20	Erase Set-Up
40	Program Set-Up
50	Clear Status Register
70	Read Status Register
90	Intelligent Identifier
B0	Erase Suspend
D0	Erase Resume/ Erase Confirm
FF	Read Array

suspend. After the WSM has completed its task, it will set the WSM Status bit to a "1", which will also allow the CUI to respond to its full command set. Note that after the WSM has returned control to the CUI, the CUI will stay in the current command state until it receives another command.

3.3.1.1 Command Function Description

Device operations are selected by writing specific commands into the CUI. Table 5 defines the available commands.

Invalid/Reserved

These are unassigned commands and should not be used. Intel reserves the right to redefine these codes for future functions.

Read Array (FFH)

This single write cycle command points the read path at the array. If the host CPU performs a CE#/OE#-controlled Read immediately following a two-write sequence that started the WSM, then the device will output Status Register contents. If the Read Array command is given after the Erase Setup command, the device will reset to read the array. A two Read Array command sequence (FFH) is required to reset to Read Array after the Program Setup command.

Intelligent Identifier (90H)

After this command is executed, the CUI points the output path to the intelligent identifier circuits. Only intelligent identifier values at addresses 0 and 1 can be read (only address A_0 is used in this mode, all other address inputs are ignored).

Read Status Register (70H)

This is one of the two commands that is executable while the WSM is operating. After this command is written, a read of the device will output the contents of the Status Register, regardless of the address presented to the device.

The device automatically enters this mode after program or erase has completed.

Clear Status Register (50H)

The WSM can only set the Program Status and Erase Status bits in the Status Register to "1", it cannot clear them to "0".

Two reasons exist for operating the Status Register in this fashion. The first is synchronization. Since the WSM does not know when the host CPU has read the Status Register, it would not know when to clear the status bits. Secondly, if the CPU is programming a string of bytes, it may be more efficient to query the Status Register after programming the string. Thus, if any errors exist while programming the string, the Status Register will return the accumulated error status.

Table 6. Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle		
	8	Oper	Addr	Data	Oper	Addr	Data
Read Array	1	Write	X	FFH			
Intelligent Identifier	2,4	Write	X	90H	Read	IA	IID
Read Status Register	3	Write	X	70H	Read	X	SRD
Clear Status Register		Write	X	50H			
Word/Byte Write	6,7	Write	WA	40H	Write	WA	WD
Alternate Word/Byte Write	6,7	Write	WA	10H	Write	WA	WD
Block Erase/Confirm	5	Write	BA	20H	Write	BA	D0H
Erase Suspend/Resume		Write	X	B0H	Write	X	D0H

ADDRESS
BA = Block Address
IA = Identifier Address
WA = Write Address
X = Don't Care

DATA
SRD = Status Register Data
IID = Identifier Data
WD = Write Data

NOTES:
1. Bus operations are defined in Tables 2 and 3.
2. IA = Identifier Address: $A_0 = 0$ for manufacturer code, $A_0 = 1$ for device code.
3. SRD – Data read from Status Register.
4. IID = Intelligent Identifier Data. Following the Intelligent Identifier command, two Read operations access manufacturer and device codes.
5. BA = Address within the block being erased.
6. WA = Address to be written. WD = Data to be written at location WD.
7. Either 40H or 10H commands is valid.
8. When writing commands to the device, the upper data bus [DQ_8–DQ_{15}] = X (28F400 only) which is either V_{CC} or V_{SS}, to minimize current draw.

Program Setup (40H or 10H)

This command simply sets the CUI into a state such that the next write will load the Address and Data registers. After this command is executed, the outputs default to the Status Register. A two Read Array command sequence (FFH) is required to reset to Read Array after the Program Setup command.

Program

The second write after the Program Setup command, will latch addresses and data. Also, the CUI initiates the WSM to begin execution of the program algorithm. The device outputs Status Register data when OE# is enabled. A Read Array command is required after programming, to read array data.

Erase Setup (20H)

Prepares the CUI for the Erase Confirm command. No other action is taken. If the next command is not an Erase Confirm command, then the CUI will set both the Program Status and Erase Status bits of the Status Register to a "1", place the device into the Read Status Register state, and wait for another command.

Erase Confirm (D0H)

If the previous command was an Erase Setup command, then the CUI will enable the WSM to erase, at the same time closing the address and data latches, and respond only to the Read Status Register and Erase Suspend commands. While the WSM is executing, the device will output Status Register data when OE# is toggled low. Status Register data can only be updated by toggling either OE# or CE# low.

Erase Suspend (B0H)

This command is only valid while the WSM is executing an Erase operation, and therefore will only be responded to during an Erase operation. After this command has been executed, the CUI will set an output that directs the WSM to suspend Erase operations, and then respond only to Read Status Register or to the Erase Resume commands. Once the WSM has reached the Suspend state, it will set an output into the CUI which allows the CUI to respond to the Read Array, Read Status Register, and Erase Resume commands. In this mode, the CUI will not respond to any other commands. The WSM will also set the WSM Status bit to a "1". The WSM will continue to run, idling in the SUSPEND state, regardless of the state of all input control pins except RP#, which will immediately shut down the WSM and the remainder of the chip, if it is made active. During a Suspend operation, the data and address latches will remain closed, but the address pads are able to drive the address into the read path.

Erase Resume (D0H)

This command will cause the CUI to clear the Suspend state and clear the WSM Status Bit to a "0", but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect under any other conditions.

3.3.2 STATUS REGISTER

The device contains a Status Register which may be read to determine when a Program or Erase operation is complete, and whether that operation completed successfully. The Status Register may be read at any time by writing the Read Status command to the CUI. After writing this command, all subsequent Read operations output data from the Status Register until another command is written to the CUI. A Read Array command must be written to the CUI to return to the read array mode.

The Status Register bits are output on DQ[0:7], whether the device is in the byte-wide (x8) or word-wide (x16) mode. In the word-wide mode the upper byte, DQ[8:15], is set to 00H during a Read Status command. In the byte-wide mode, DQ[8:14] are tri-stated and DQ_{15}/A_{-1} retains the low order address function.

Important: *The contents of the Status Register are latched on the falling edge of OE# or CE#, whichever occurs last in the read cycle.* This prevents possible bus errors which might occur if the contents of the Status Register change while reading the Status Register. CE# or OE# must be toggled with each subsequent status read, or the completion of a Program or Erase operation will not be evident from the Status Register.

When the WSM is active, this register will indicate the status of the WSM, and will also hold the bits indicating whether or not the WSM was successful in performing the desired operation.

3.3.2.1 Clearing the Status Register

The WSM sets status bits "3" through "7" to "1", and clears bits "6" and "7" to "0", but cannot clear status bits "3" through "5" to "0". Bits 3 through 5 can only be cleared by the controlling CPU through the use of the Clear Status Register command. These bits can indicate various error conditions. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several bytes or erasing multiple blocks in sequence). The Status Register may then be read to determine if an error occurred during that programming or erasure series. This adds flexibility to the way the device may be programmed or erased. To clear the Status Register, the Clear Status Register command is written to the CUI. Then, any other command may be issued to the CUI. Note, again, that before a read cycle can be initiated, a Read Array command must be written to the CUI to specify whether the read data is to come from the Memory Array, Status Register, or Intelligent Identifier.

3.3.3 PROGRAM MODE

Programing is executed using a two-write sequence. The Program Setup command is written to the CUI followed by a second write which specifies the address and data to be programmed. The WSM will execute a sequence of internally timed events to:

1. Program the desired bits of the addressed memory word or byte.
2. Verify that the desired bits are sufficiently programmed.

Programming of the memory results in specific bits within a byte or word being changed to a "0".

If the user attempts to program "1"s, there will be no change of the memory cell content and no error occurs.

Similar to erasure, the Status Register indicates whether programming is complete. While the program sequence is executing, bit 7 of the Status Register is a "0". The Status Register can be polled by toggling either CE# or OE# to determine when the program sequence is complete. Only the Read Status Register command is valid while programming is active.

Table 7. Status Register Bit Definition

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

	NOTES:
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Write State Machine bit must first be checked to determine Byte/Word program or Block Erase completion, before the Program or Erase Status bits are checked for success.
SR.6 = ERASE-SUSPEND STATUS (ESS) 1 = Erase Suspended 0 = Erase In Progress/Completed	When Erase Suspend is issued, WSM halts execution and sets both WSMS and ESS bits to "1". ESS bit remains set to "1" until an Erase Resume command is issued.
SR.5 = ERASE STATUS 1 = Error In Block Erasure 0 = Successful Block Erase	When this bit is set to "1", WSM has applied the maximum number of erase pulses to the block and is still unable to successfully verify block erasure.
SR.4 = PROGRAM STATUS 1 = Error in Byte/Word Program 0 = Successful Byte/Word Program	When this bit is set to "1", WSM has attempted but failed to program a byte or word.
SR.3 = V_{PP} STATUS 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK	The V_{PP} Status bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP} level only after the Byte Write or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. The V_{PP} Status bit is not guaranteed to report accurate feedback between V_{PPLK} and V_{PPH}.
SR.2–SR.0 = RESERVED FOR FUTURE ENHANCEMENTS	These bits are reserved for future use and should be masked out when polling the Status Register.

When programming is complete, the status bits, which indicate whether the Program operation was successful, should be checked. If bit 3 is set to a "1", then V_{PP} was not within acceptable limits, and the WSM did not execute the programming sequence. If the Program operation fails, Bit 4 of the Status Register will be set within 3.3 ms as determined by the timeout of the WSM.

The Status Register should be cleared before attempting the next operation. Any CUI instruction can follow after programming is completed; however, reads from the Memory Array, Status Register, or Intelligent Identifier cannot be accomplished until the CUI is given the Read Array command.

3.3.4 ERASE MODE

Erasure of a single block is initiated by writing the Erase Setup and Erase Confirm commands to the CUI, along with the addresses identifying the block to be erased. These addresses are latched internally when the Erase Confirm command is issued. Block erasure results in all bits within the block being set to "1".

The WSM will execute a sequence of internally timed events to:

1. Program all bits within the block to "0".
2. Verify that all bits within the block are sufficiently programmed to "0".
3. Erase all bits within the block.
4. Verify that all bits within the block are sufficiently erased.

While the erase sequence is executing, bit 7 of the Status Register is a "0".

When the Status Register indicates that erasure is complete, the status bits, which indicate whether the Erase operation was successful, should be checked. If the Erase operation was unsuccessful, bit 5 of the Status Register will be set to a "1", indicating an Erase Failure. If V_{PP} was not within acceptable limits after the Erase Confirm command is issued, the WSM will not execute an erase sequence; instead, bit 5 of the Status Register is set to a "1" to indicate an Erase Failure, and bit 3 is set to a "1" to identify that V_{PP} supply voltage was not within acceptable limits.

The Status Register should be cleared before attempting the next operation. Any CUI instruction can follow after erasure is completed; however, reads from the Memory Array, Status Register, or Intelligent Identifier cannot be accomplished until the CUI is given the Read Array command.

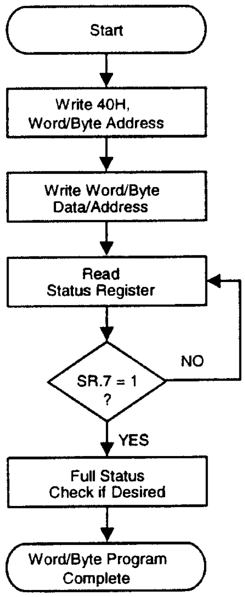
3.3.4.1 Suspending and Resuming Erase

Since an Erase operation requires on the order of seconds to complete, an Erase Suspend command is provided to allow erase-sequence interruption in order to read data from another block of the memory. Once the erase sequence is started, writing the Erase Suspend command to the CUI requests that the WSM pause the erase sequence at a pre-determined point in the erase algorithm. The Status Register must then be read to determine if the Erase operation has been suspended.

At this point, a Read Array command can be written to the CUI in order to read data from blocks other than that which is being suspended. The only other valid command at this time is the Erase Resume command or Read Status Register command.

During erase suspend mode, the chip can go into a pseudo-standby mode by taking CE# to V_{IH}, which reduces active current draw.

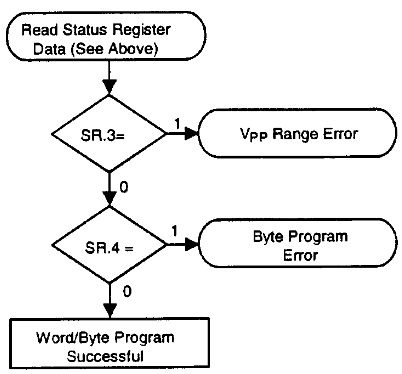
To resume the Erase operation, the chip must be enabled by taking CE# to V_{IL}, then issuing the Erase Resume command. When the Erase Resume command is given, the WSM will continue with the erase sequence and complete erasing the block. As with the end of a standard erase operation, the Status Register must be read, cleared, and the next instruction issued in order to continue.



Bus Operation	Command	Comments
Write	Setup Program	Data = 40H Addr = Word/Byte to Program
Write	Program	Data = Data to Program Addr = Location to Program
Read		Status Register Data Toggle CE# or OE# to Update SRD.
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent Word/Byte Writes.
SR Full Status Check can be done after each Word/Byte Write, or after a sequence of Word/Byte Writes.
Write FFH after the last write operation to reset device to read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4 1 = V_{PP} Byte Program Error

SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine.

SR.4 is only cleared by the Clear Status Register Command, in cases where multiple bytes are programmed before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

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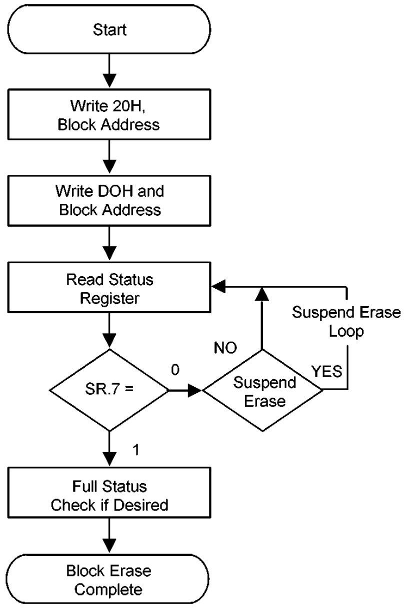
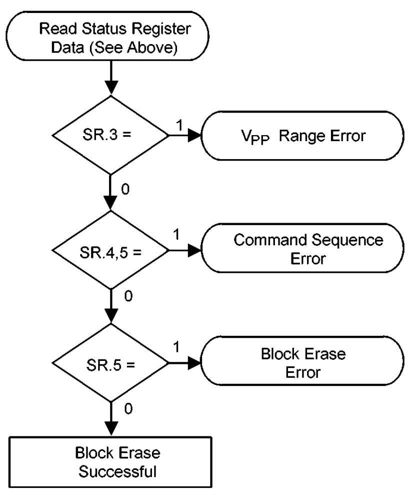
Figure 4. Automated Word/Byte Programming Flowchart



Bus Operation	Command	Comments
Write	Erase Setup	Data = 20H Addr = Within Block to be Erased
Write	Erase Confirm	Data = D0H Addr = Within Block to be Erased
Read		Status Register Data Toggle CE# or OE# to Update Status Register
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent block erasures.
Full Status Check can be done after each block erase, or after a sequence of block erasures.
Write FFH after the last operation to reset device to read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4,5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error

SR.3 MUST be cleared, if set during an erase attempt, before further attempts are allowed by the Write State Machine.

SR.5 is only cleared by the Clear Status Register Command, in cases where multiple blocks are erase before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

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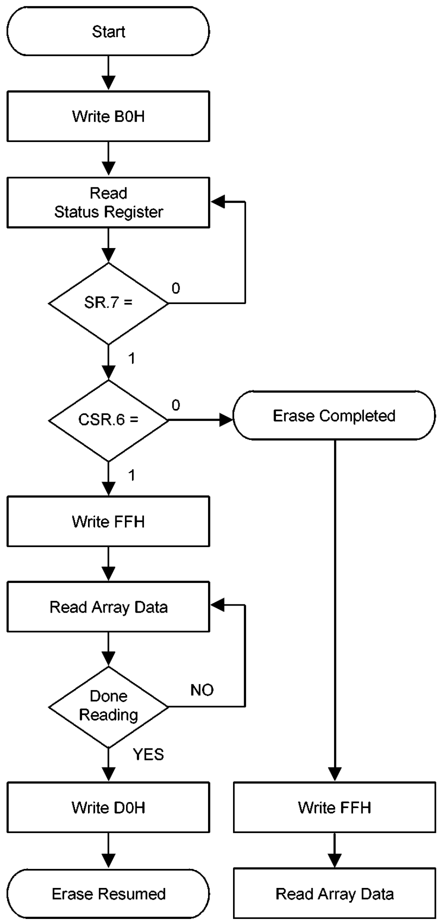
Figure 5. Automated Block Erase Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H Addr = X
Read		Status Register Data Toggle CE# or OE# to update SRD. Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Erase Suspended 0 = Erase Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array data from block other than the one being erased.
Write	Erase Resume	Data = D0H Addr = X

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Figure 6. Erase Suspend/Resume Flowchart

3.4 Boot Block Locking

The boot block family architecture features a hardware-lockable boot block so that the kernel code for the system can be kept secure while the parameter and main blocks are programmed and erased independently as necessary. Only the boot block can be locked independently from the other blocks.

3.4.1 $V_{PP} = V_{IL}$ FOR COMPLETE PROTECTION

For complete write protection of all blocks in the flash device, the V_{PP} programming voltage can be held low. When V_{PP} is below V_{PPLK}, any Program or Erase operation will result in a error in the Status Register.

3.4.2 WP# = V_{IL} FOR BOOT BLOCK LOCKING

When WP# = V_{IL}, the boot block is locked and any Program or Erase operation will result in an error in the Status Register. All other blocks remain unlocked in this condition and can be programmed or erased normally. Note that this feature is overridden and the boot block unlocked when RP# = V_{HH}.

3.4.3 RP# = V_{HH} OR WP# = V_{IH} FOR BOOT BLOCK UNLOCKING

Two methods can be used to unlock the boot block:

1. WP# = V_{IH}
2. RP# = V_{HH}

If both or either of these two conditions are met, the boot block will be unlocked and can be programmed or erased. The Truth Table, Table 8, clearly defines the write protection methods.

Table 8. Write Protection Truth Table for SmartVoltage Boot Block Family

V_{PP}	RP#	WP#	Write Protection Provided
V_{IL}	X	X	All Blocks Locked
$\geq V_{PPLK}$	V_{IL}	X	All Blocks Locked (Reset)
$\geq V_{PPLK}$	V_{HH}	X	All Blocks Unlocked
$\geq V_{PPLK}$	V_{IH}	V_{IL}	Boot Block Locked
$\geq V_{PPLK}$	V_{IH}	V_{IH}	All Blocks Unlocked

3.5 Power Consumption

3.5.1 ACTIVE POWER

With CE# at a logic-low level and RP# at a logic-high level, the device is placed in the active mode. Refer to the DC Characteristics table for I_{CC} current values.

3.5.2 AUTOMATIC POWER SAVINGS (APS)

Automatic Power Savings (APS) is a low-power feature during active mode of operation. The boot block flash memory family incorporates Power Reduction Control (PRC) circuitry which allows the device to put itself into a low current state when it is not being accessed. After data is read from the memory array, PRC logic controls the device's power consumption by entering the APS mode where typical I_{CC} current is less than1 mA. The device stays in this static state with outputs valid until a new location is read.

3.5.3 STANDBY POWER

With CE# at logic high level (V_{IH}), and the CUI in read mode, the memory is placed in standby mode. The Standby operation disables much of the device's circuitry and substantially reduces device power consumption. The outputs (DQ[0:15] or DQ[0:7]) are placed in a high-impedance state independent of the status of the OE# signal. When CE# is at logic-high level during erase or program functions, the devices will continue to perform the erase or program function and consume erase or program active power until erase or program is completed.

3.5.4 DEEP POWER-DOWN MODE

The SmartVoltage boot block family supports a low typical I_{CC} in deep power-down mode. The device has a RP# pin which places the device in the deep power-down mode. When RP# is at a logic-low (GND ± 0.2V), all circuits are turned off in order to save power. (Note: BYTE# pin must be at CMOS levels to achieve the most deep power-down current savings.)

During read modes, the RP# pin going low de-selects the memory and places the output drivers in a high impedance state. Recovery from the deep power-down state, requires a minimum access time of t_{PHQV}. (See the AC Characteristics table for specification numbers.)

During erase or program modes, RP# low will abort either Erase or Program operation. The contents of the memory are no longer valid as the data has been corrupted by the RP# function. As in the read mode above, all internal circuitry is turned off to achieve the power savings.

RP# transitions to V_{IL}, or turning power off to the device will clear the Status Register.

3.6 Power-Up Operation

The device is designed to offer protection against accidental block erasure or programming during power transitions. Upon power-up, the device is indifferent as to which power supply, V_{PP} or V_{CC}, powers-up first. Power supply sequencing is not required.

A system designer must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both WE# and CE# must be low for a command write, driving either signal to V_{IH} will inhibit writes to the device. The CUI architecture provides an added level of protection since alteration of memory contents can only occur after successful completion of the two-step command sequences. Finally the device is disabled until RP# is brought to V_{IH}, regardless of the state of its control inputs. By holding the device in reset (RP# connected to system PowerGood) during power up/down, invalid bus conditions that may occur can be masked. This feature provides yet another level of memory protection.

3.6.1 RP# CONNECTED TO SYSTEM RESET

The use of RP# during system reset is important with automated write/erase devices. When the system comes out of reset it expects to read from the flash memory. Automated flash memories provide status information when accessed during writes/erase modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization would not occur because the flash memory would be providing the status information instead of array data. Intel's flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application RP# is controlled by the same RESET# signal that resets the system CPU.

3.7 Power Supply Decoupling

Flash memory's power switching characteristics require careful device decoupling methods. System designers should consider three supply current issues:

1. Standby current levels (I_{CCS})
2. Active current levels (I_{CCR})
3. Transient peaks produced by falling and rising edges of CE#.

Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress these transient voltage peaks. Each flash device should have a 0.1 μF ceramic capacitor connected between each V_{CC} and GND, and between its V_{PP} and GND. These high frequency, inherently low inductance capacitors should be placed as close as possible to the package leads.

3.7.1 V_{PP} TRACE ON PRINTED CIRCUIT BOARDS

Writing to flash memories while they reside in the target system, requires special consideration of the V_{PP} power supply trace by the printed circuit board designer. The V_{PP} pin supplies the flash memory cells current for programming and erasing. One should use similar trace widths and layout considerations given to the V_{CC} power supply trace. Adequate V_{PP} supply traces, and decoupling capacitors placed adjacent to the component, will decrease spikes and overshoots.

3.7.2 V_{CC}, V_{PP} AND RP# TRANSITIONS

The CUI latches commands as issued by system software and is not altered by V_{PP} or CE# transitions or WSM actions. Its default state upon power-up, after exit from deep power-down mode, or after V_{CC} transitions above V_{LKO} (Lockout voltage), is read array mode.

After any Word/Byte Write or Block Erase operation is complete and even after V_{PP} transitions down to V_{PPLK}, the CUI must be reset to read array mode via the Read Array command when accesses to the flash memory are desired.

4.0 ABSOLUTE MAXIMUM RATINGS*

Operating Temperature

During Read .... −40°C to +125°C

During Block Erase and Word/Byte Write .... −40°C to +125°C

Temperature Under Bias ..... −40°C to +125°C

Storage Temperature .... −65°C to +125°C

Voltage on Any Pin

(except V_{CC}, V_{PP}, A_9 and RP#) with Respect to GND .... −2.0V to +7.0V(1)

Voltage on Pin RP# or Pin A_9 with Respect to GND .... −2.0V to +13.5V(1,2)

V_{PP} Program Voltage with Respect to GND during Block Erase and Word/Byte Write ..... −2.0V to +14.0V(1,2)

V_{CC} Supply Voltage with Respect to GND .... −2.0V to +7.0V(1)

Output Short Circuit Current .... 100 mA (3)

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Minimum DC voltage is −0.5V on input/output pins. During transitions, this level may undershoot to −2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
2. Maximum DC voltage on V_{PP} may overshoot to +14.0V for periods <20ns. Maximum DC voltage on RP# or A_9 may overshoot to 13.5V for periods <20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

5.0 OPERATING CONDITIONS

Table 9. Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Notes	Min	Max	Units
T_A	Operating Temperature		−40	+125	°C
V_{CC}	V_{CC} Supply Voltage (10%)		4.50	5.50	Volts

5.1 Applying V_{CC} Voltages

If the V_{CC} ramp rate is greater than 0.01 V/µs, a delay of 2 µs is required before any device operation can be initiated. This includes array or status reads, command writes and program or erase operations. The 2 µs are measured beginning from the time V_{CC} reaches V_{CCMIN} (4.5V). This delay is not tied to the operation of the reset input. It is recommended that the device be held in reset (RP# = GND) while V_{CC} is less than V_{CCMIN}.

If the V_{CC} ramp rate is less than 0.01 V/µs no delay is required once V_{CC} has reached V_{CCMIN}.

5.2 DC Characteristics

Table 10. DC Characteristics: Automotive Temperature Operation

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Conditions
I_{IL}	Input Load Current	1			±5.0	μA	$V_{CC} = V_{CC}$MAX $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1			±10	μA	$V_{CC} = V_{CC}$ MAX $V_{IN} = V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1,3		0.8	2.5	mA	$V_{CC} = V_{CC}$ MAX CE# = RP# = BYTE# = V_{IH}
				70	250	μA	$V_{CC} = V_{CC}$ MAX CE# = RP# = WP# = V_{CC} ± 0.2V
I_{CCD}	V_{CC} Deep Power-Down Current	1		0.2	105	μA	$V_{CC} = V_{CC}$ MAX $V_{IN} = V_{CC}$ or GND RP# = GND ± 0.2V
I_{CCR}	V_{CC} Read Current for Word or Byte	1,5,6		50	65	mA	CMOS $V_{CC} = V_{CC}$ MAX CE = V_{IL} f = 10 Mhz (5V) 5 Mhz (3.3V) I_{OUT} = 0 mA Inputs = GND ± 0.2V or V_{CC} ± 0.2V
				55	70	mA	TTL $V_{CC} = V_{CC}$ MAX CE# = V_{IL} f = 10 MHz I_{OUT} = 0 mA Inputs = V_{IL} or V_{IH}
I_{CCW}	V_{CC} Write Current for Word or Byte	1,4		25	50	mA	Word/Byte Program in Progress $V_{PP} = V_{PPH}1$ (at 5V)
				20	45	mA	Word/Byte Program in Progress $V_{PP} = V_{PPH}2$ (at 12V)

Table 10. DC Characteristics: Automotive Temperature Operation (Continued)

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Conditions
I_{CCE}	V_{CC} Erase Current	1,4		22	45	mA	Block Erase in Progress $V_{PP} = V_{PPH}1$ (at 5V)
				18	40	mA	Block Erase in Progress $V_{PP} = V_{PPH}2$ (at 12V)
I_{CCES}	V_{CC} Erase Suspend Current	1,2		5	12.0	mA	CE# = V_{IH} Block Erase Suspend $V_{PP} = V_{PPH}1$ (at 5V)
I_{PPS}	V_{PP} Standby Current	1		± 5	± 15	μA	$V_{PP} \leq V_{CC}$
I_{PPD}	V_{PP} Deep Power-down Current	1		0.2	10	μA	RP# = GND ± 0.2V
I_{PPR}	V_{PP} Read Current	1		50	200	μA	$V_{PP} > V_{CC}$
I_{PPW}	V_{PP} Write Current for Word/Byte	1		13	30	mA	$V_{PP} = V_{PPH}$ Word Write in Progress $V_{PP} = V_{PPH}1$ (at 5V)
				8	25	mA	$V_{PP} = V_{PPH}$ Word Write in Progress $V_{PP} = V_{PPH}2$ (at 12V)
I_{PPE}	V_{PP} Erase Current	1		15	25	mA	$V_{PP} = V_{PPH}$ Block Erase in Progress $V_{PP} = V_{PPH}1$ (at 5V)
				10	20	mA	$V_{PP} = V_{PPH}$ Block Erase in Progress $V_{PP} = V_{PPH}2$ (at 12V)
I_{PPES}	V_{PP} Erase Suspend Current	1		50	200	μA	$V_{PP} = V_{PPH}$ Block Erase Suspend in Progress
$I_{RP\#}$	RP# Boot Block Unlock Current	1,4			500	μA	RP# = V_{HH} V_{PP} = 12V
I_{ID}	A_9 Intelligent Identifier Current	1,4			500	μA	$A_9 = V_{ID}$
V_{ID}	A_9 Intelligent Identifier Voltage		11.4		12.6	V	
V_{IL}	Input Low Voltage		−0.5		0.8	V	

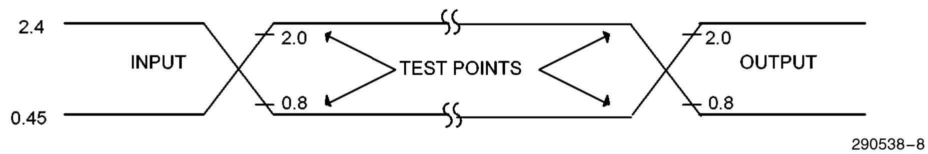
Table 10. DC Characteristics: Automotive Temperature Operation (Continued)

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Conditions
V_{IH}	Input High Voltage		2.0		V_{CC} ± 0.5V	V	
V_{OL}	Output Low Voltage (TTL)				0.45	V	$V_{CC} = V_{CC}MIN$ I_{OL} = 5.8 mA V_{PP} = 12V
$V_{OH}1$	Output High Voltage (TTL)		2.4			V	$V_{CC} = V_{CC}$ MIN I_{OH} = −1.5 mA
$V_{OH}2$	Output High Voltage (CMOS)		V_{CC} −.4V			V	$V_{CC} = V_{CC}$ MIN I_{OH} = −100 μA
V_{PPLK}	V_{PP} Lock−Out Voltage	3	0.0		1.5	V	Complete Write Protection
$V_{PPH}1$	V_{PP} (Program/Erase Operations)		4.5		5.5	V	V_{PP} at 5V
$V_{PPH}2$	V_{PP} (Program/Erase Operations)		11.4		12.6	V	V_{PP} at 12V
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.0			V	
V_{HH}	RP# Unlock Voltage		11.4		12.6	V	Boot Block Write/Erase V_{PP} = 12V

Table 11. Capacitance (T_A = 25°C, f = 1 MHz)

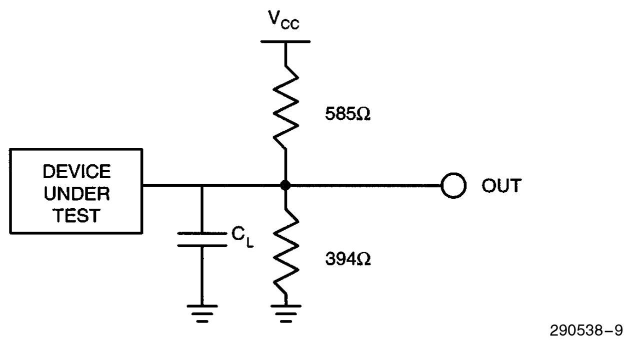
Symbol	Parameter	Note	Type	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	8	pF	V_{IN} = 0V
C_{OUT}	Ouput Capacitance	4	10	12	pF	V_{OUT} = 0V

NOTES:
1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, T = 25°C. These currents are valid for all product versions (packages and speeds).
2. I_{CCES} is specified with the device de-selected. If the devices is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Block erases and word/byte writes are inhibited when V_{PP} = V_{PPLK}, and not guaranteed in the range between $V_{PPH}1$ and V_{PPLK}.
4. Sampled, not 100% tested.
5. Automatic Power Savings (APS) reduces I_{CCR} to less than 1 mA typical, in static operation.
6. CMOS Inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL Inputs are either V_{IL} or V_{IH}.



NOTE:
AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.45 V_{TTL}) for a logic "0." Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) $\leq$ 10 ns.

Figure 7. 7V Inputs and Measurement Points



NOTE:
C_L = 100 pF, includes Jig Capacitance

Figure 8. 5V Standard Test Configuration

5.3 AC Characteristics

Table 12. AC Characteristics: Read Only Operations(1) (Automotive Temperature)

Symbol	Parameter	Note	Min	Max	Unit
t_{AVAV}	Read Cycle Time		80		ns
t_{AVQV}	Address to Output Delay			80	ns
t_{ELQV}	CE# to Output Delay	2		80	ns
t_{PHQV}	RP# to Output Delay			550	ns
t_{GLQV}	OE# to Output Delay	2		40	ns
t_{ELQX}	CE# to Output in Low Z	3	0		ns
t_{EHQZ}	CE# to Output in High Z	3		30	ns
t_{GLQX}	OE# to Output in Low Z	3	0		ns
t_{GHQZ}	OE# to Output in High Z	3		30	ns
t_{OH}	Output Hold from Address CE#, or OE# Change Whichever Occurs First	3	0	0	ns
t_{ELFL} t_{ELFH}	CE# Low to BYTE High or Low	3		5	ns
t_{AVFL}	Address to BYTE# High or Low	3		5	ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3,4		80	ns
t_{FLQZ}	BYTE# low to Output in High Z	3		30	ns

NOTES:
1. See AC Input/Output Reference Waveform for timing measurements.
2. OE# may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of CE# without impact on t_{CE}.
3. Sampled, but not 100% tested.
4. t_{FLQV}, BYTE# switching low to valid output delay will be equal to t_{AVQV}, measured from the time DQ_{15}/A_{-1} becomes valid.
5. See 5V Standard Test Configuration. (Figure 9)

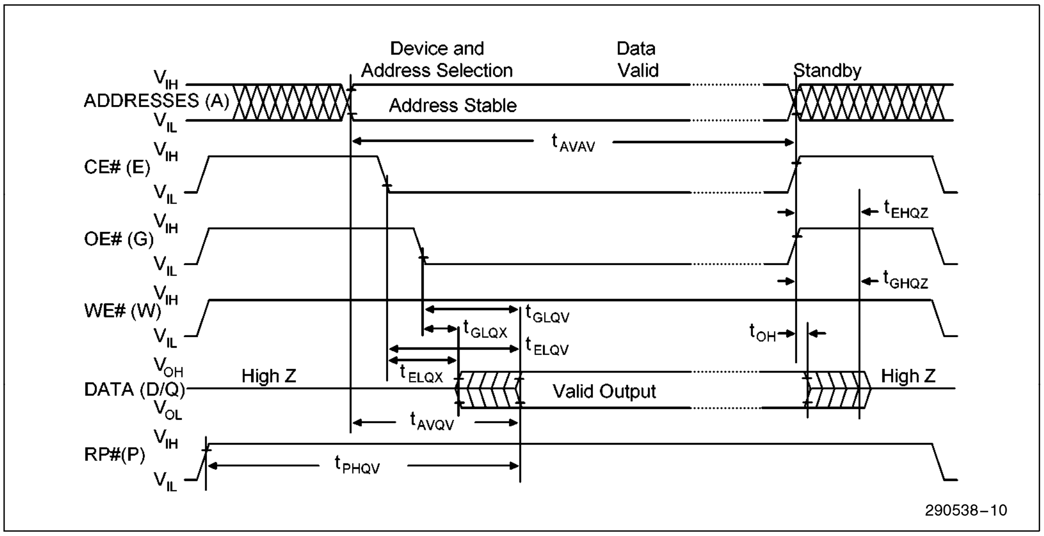


Figure 9. AC Waveforms for Read Operations

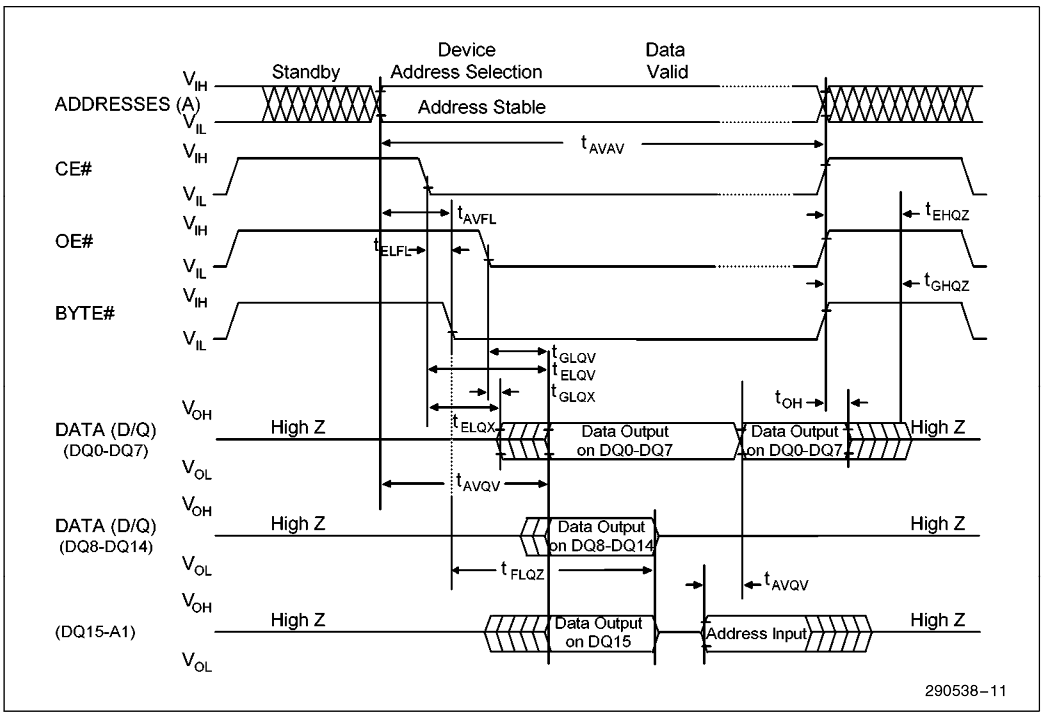


Figure 10. BYTE# Timing Diagram for Both Read and Write Operations with V_{CC} at 5V

Table 13. AC Characteristics: WE#—Controlled Write Operations(1) (Automotive Temperature)

Symbol	Parameter	Notes	Min	Max	Unit
t_{AVAV}	Write Cycle Time		80		ns
t_{PHWL}	RP# High Recovery to WE# Going Low		450		ns
t_{ELWL}	CE# Setup to WE# Going Low		0		ns
t_{PHHWH}	Boot Block Lock Setup to WE# Going High	6,8	100		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	5,8	100		ns
t_{AVWH}	Address Setup to WE# Going High	3	60		ns
t_{DVWH}	Data Setup to WE# Going High	4	60		ns
t_{WLWH}	WE# Pulse Width		60		ns
t_{WHDX}	Data Hold Time from WE# High	4	0		ns
t_{WHAX}	Address Hold Time from WE# High	3	10		ns
t_{WHEH}	CE# Hold Time from WE# High		10		ns
t_{WHWL}	WE# Pulse Width High		20		ns
t_{WHQV1}	Duration of Word/Byte Write Operation	2,5	7		µs
t_{WHQV2}	Duration of Erase Operation (Boot)	2,5,6	0.4		s
t_{WHQV3}	Duration of Erase Operation (Parameter)	2,5	0.4		s
t_{WHQV4}	Duration of Erase Operation (Main)	2,5	0.7		s
t_{QWL}	V_{PP} Hold from Valid SRD	5,8	0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD	6,8	0		ns
t_{PHBR}	Boot-Block Relock Delay	7,8		100	ns

NOTES:
1. Read timing characteristics during write and erase operations are the same as during read-only operations. Refer to AC Characteristics during read mode.
2. The on-chip WSM completely automates Program/Erase operations; Program/Erase algorithms are now controlled internally which includes verify and margining operations.
3. Refer to command definition table for valid A_{IN}.
4. Refer to command definition table for valid D_{IN}.
5. Program/Erase durations are measured to valid SRD data (successful operation, SR.7 = 1)
6. For boot block Program/Erase, RP# should be held at V_{HH} or WP# should be held at V_{IH} until operation completes successfully.
7. Time t_{PHBR} is required for successful relocking of the boot block.
8. Sampled, but not 100% tested.
9. V_{PP} at 5.0V.
10. V_{PP} at 12.0V.
11. See 5V Standard Test Configuration.

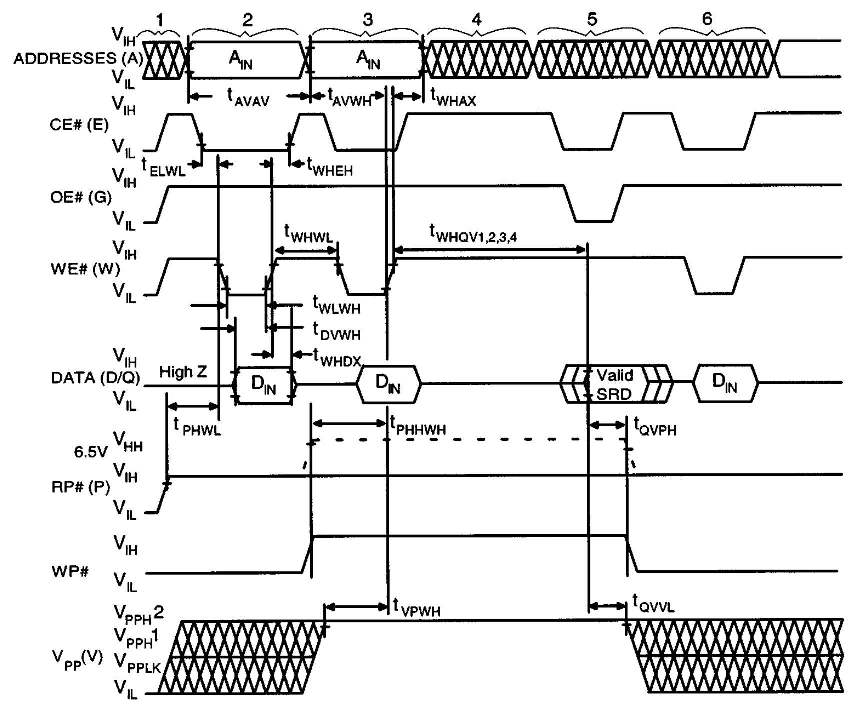


Figure 11. AC Waveforms for Write and Erase Operations (WE#-Controlled Writes)

Table 14. AC Characteristics: CE#—Controlled Write Operations (1,12)

Symbol	Parameter	Notes	Min	Max	Unit
t_{AVAV}	Write Cycle Time		80		ns
t_{PHEL}	RP# High Recovery to CE# Going Low		450		ns
t_{WLEL}	WE# Setup to CE# Going Low		0		ns
t_{PHHEH}	Boot Block Lock Setup to CE# Going High	6,8	100		ns
t_{VPEH}	V_{PP} Setup to CE# Going High	5,8	100		ns
t_{AVEH}	Address Setup to CE# Going High		60		ns
t_{DVEH}	Data Setup to CE# Going High	3	60		ns
t_{ELEH}	CE# Pulse Width	4	60		ns
t_{EHDX}	Data Hold Time from CE# High		0		ns
t_{EHAX}	Address Hold Time from CE# High	4	10		ns
t_{EHWH}	WE# Hold Time from CE# High	3	10		ns
t_{EHEL}	CE# Pulse Width High		20		ns
t_{EHQV1}	Duration of Word/Byte Write Operation	2,5	7		µs
t_{EHQV2}	Duration of Erase Operation (Boot)	2,5,6	0.4		s
t_{EHQV3}	Duration of Erase Operation (Parameter)	2,5	0.4		s
t_{EHQV4}	Duration of Erase Operation (Main)	2,5	0.7		s
t_{QWL}	V_{PP} Hold from Valid SRD	5,8	0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD	6,8	0		ns
t_{PHBR}	Boot-Block Relock Delay	7,8		100	ns

NOTES:

See WE# Controlled Write Operations for notes 1 through 11.

12. Chip-Enable controlled writes: Write operations are driven by the valid combination of CE# and WE# in systems where CE# defines the write pulse-width (within a longer WE# timing waveform), all set-up, hold and inactive WE# times should be measured relative to the CE# waveform.

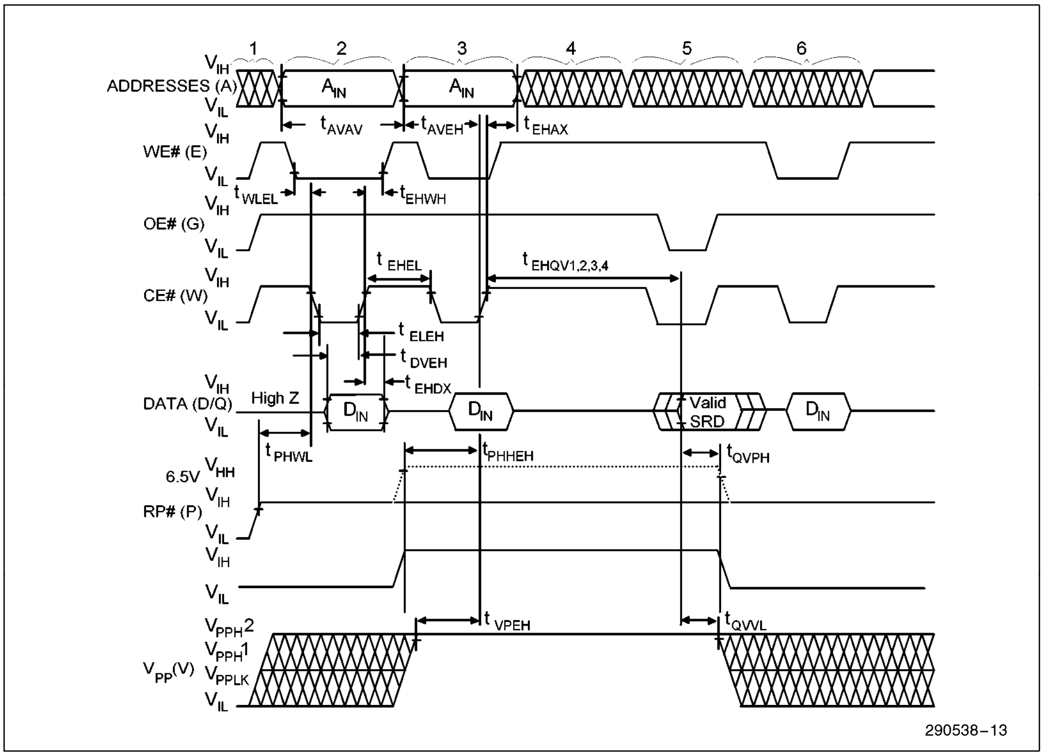


Figure 12. Alternate AC Waveforms for Write and Erase Operations (CE#-Controlled Writes)

Table 15. AC Characteristics: Reset Timings(1)

Symbol	Parameter	Notes	Min	Max	Unit
t_{PLPH}	Reset Pulse Duration		60		ns
t_{PLQZ}	RP# Low to Output in High Z			60	ns

NOTE:
1. Refer to Figure 13 for waveform

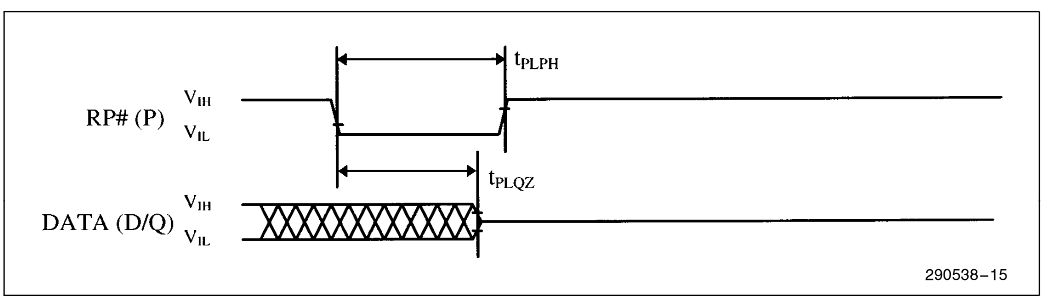
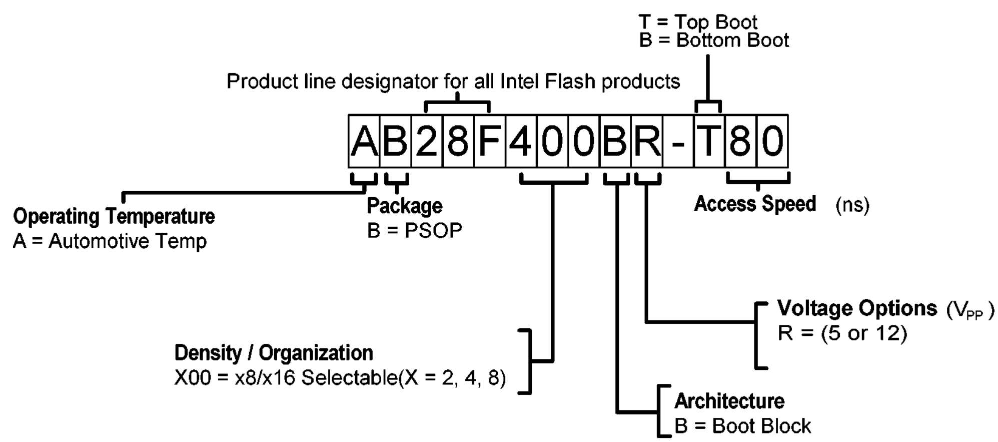


Figure 13. Reset Waveforms

6.0 ADDITIONAL INFORMATION

6.1 Ordering Information



290538–14

VALID COMBINATIONS:
AB28F400BR–T80 AB28F400BR–B80

6.2 References

Order Number	Document
292130	AB-57 "Boot Block Architecture for Safe Firmware Updates"
292154	AB-60 "2/4/8-Mbit SmartVoltage Boot Block Flash Memory Family"
292098	AP-363 "Extended Flash BIOS Concepts for Portable Computers"
292148	AP-604 "Using Intel's Boot Block Flash Memory Parameter Blocks to Replace EEPROM"
290448	28F002/200BX-T/B 2-Mbit Boot Block Flash Memory Datasheet
290449	28F002/200BL-T/B 2-Mbit Low Power Boot Block Flash Memory Datasheet
290450	28F004/400BL-T/B 4-Mbit Low Power Boot Block Flash Memory Datasheet
290451	28F004/400BX-T/B 4-Mbit Boot Block Flash Memory Datasheet

6.3 Revision History

Number	Description
−001	Initial release of datasheet
−002	Changed RP# AC Characteristic Changed V_{LKO} to 3.5V
−003	Changed definition of t_{5VPH} in Section 5.1 Changed I_{CCS}, I_{CCD} and V_{LKO} specifications Added Table 11, I/O capacitance Added rise and fall time limits to Figure 7 Changed t_{PHEL} from a Max timing to a Min
−004	Increased maximum program/erase cycles for parameter blocks to 30,000 Corrected Flowchart in Figures 4 and 5 Reformatted Sections 5.1 Increased I_{IL} to $\pm 5\ \mu A$ Removed Table 15. Erase and Program Timings Added new Table 15. Reset Timings and Figure 13 Reset Waveforms