82527

SPECIFICATION UPDATE

Release Date: July, 1996

Order Number 272876-001

The 82527 may contain design defects or errors known as errata. Characterized errata that may cause the 82527's behavior to deviate from published specifications are documented in this specification update.

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
07/01/96	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This is the first release of the 82527 Specification Update. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published.

Affected Documents/Related Documents

Title	Order
82527 Serial Communications Controller Controller Area Network Protocol	272250-006

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 82527 product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	#	#	#			
9600001	C			7	NoFix	Fast Read Data Corruption

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
	#	#	#			
						None for this revision of this specification update.

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
				None for this revision of this specification update.

IDENTIFICATION INFORMATION

Markings

AN82527, AS82527

ERRATA

9600001. Fast Read Data Corruption

PROBLEM: Under certain conditions, it is possible when performing “fast reads” of the 82527 that invalid data can be read or an entire message object can be overwritten. This problem affects all bus interface modes of the 82527 (mode 0, 1, 2, 3) except the serial interface or SPI-compatible mode. The problem is encountered when using host CPUs that cannot lengthen the bus cycle to meet the read timing requirements of the 82527 (i.e., no READY or DSACK0#). With these CPUs, the double read operation is typically used to access low-speed register data, where the first read operation (a dummy read) is to the low-speed register address, followed by a second read (valid data) of the high-speed read register.

For mode 0 and mode 1 (Intel multiplexed modes), the control signals ALE, RD# and WR# are used to define the address and whether the cycle is a data read or write operation. The ALE signal is commonly used to latch the address information and generate a CS# signal to the 82527. The problem occurs in this configuration when the next cycle ALE is asserted before CS# of the current cycle becomes invalid. This circumstance presents a problem only when CS# is active and the next cycle’s ALE occurs less than 1.5 t_{MCLK} after the current cycle’s RD# low. ($t_{MCLK} = t_{OSC}/[(1 + DSC\ bit) + DMC\ bit]$ where DSC = Divide System Clock, DMC = Divide Memory Clock.

When performing “fast reads” associated with the double-read operation in mode 0 or 1, one of the following two conditions must be true:

1) The time from RD# low of the current cycle to the next ALE must be greater than 1.5 t_{MCLK}, or

2) The CS# signal to the 82527 must be inactive before the next occurrence of an ALE, when the time from the RD# low of the current cycle to the next cycle’s CS# active is less than 1.5 t_{MCLK}.

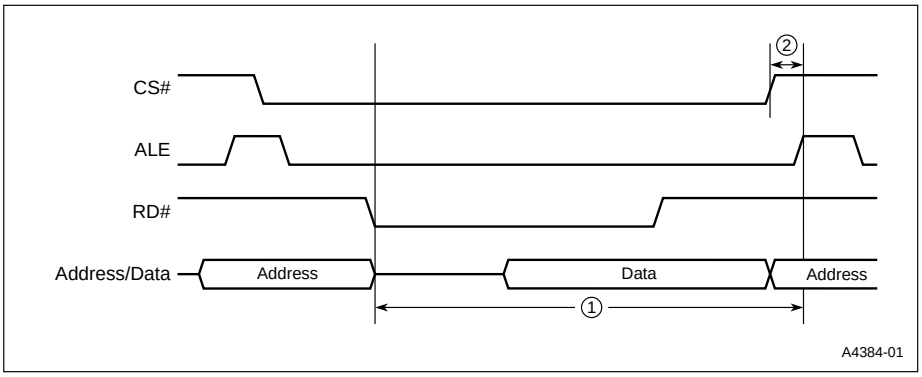


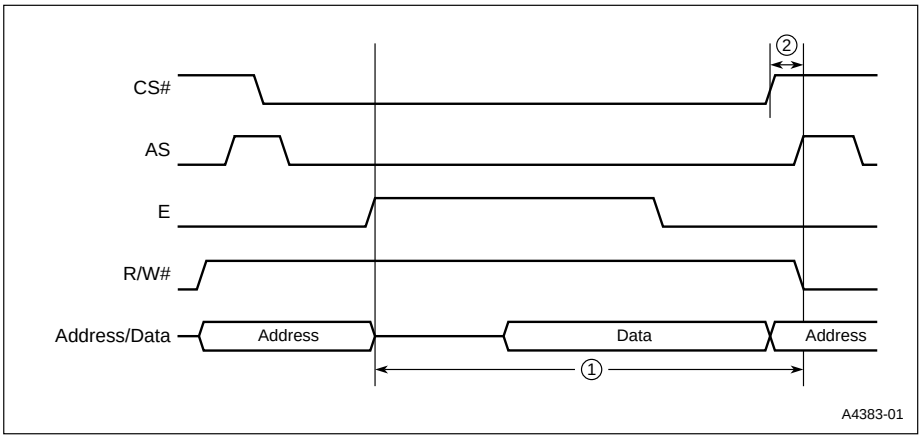
Figure 1: Bus cycle for Mode 0 or Mode 1 Operation (Read Cycle)

For mode 2, the control signals AS, R/W#, and E are used to define the address, to specify whether the cycle is a data read or write operation, and to synchronize the memory accesses. The AS signal is commonly used to latch the address information and generate a CS# signal to the 82527. The problem, as outlined for modes 0 and 1, occurs when the next cycle's AS is asserted before CS# of the current cycle becomes invalid. This circumstance presents a problem only if the next cycle's AS occurs in less than 1.5 t_{MCLK} after the current cycle's E low while CS# is still active.

For mode 2 operation, one of the following two criteria must be true:

1) The time from E high of the current cycle to the next AS must be equal to or greater than 1.5 t_{MCLK}, or

2) The CS# signal to the 82527 must be inactive before the next occurrence of an AS, when the time from E high of the current cycle to the next cycle CS# active is less than 1.5 t_{MCLK}.



(Figure 2): Bus Cycle for Mode 2 Operation (Read Cycle)

For mode 3 synchronous operation, there is no ALE or AS signal. Mode 3 is the demultiplexed mode of the 82527. For this mode, the address information must be present through the entire cycle. However, when performing fast read operations, similar considerations as the other modes must be observed to prevent problems when performing reads from the 82527.

For mode 3 synchronous operation, one of the following two criteria must be true:

1) The time from E high of the current cycle to CS# invalid must be equal to or greater than 1.5 t_{MCLK}, or

2) Address information must remain valid on the bus until after CS# goes inactive.

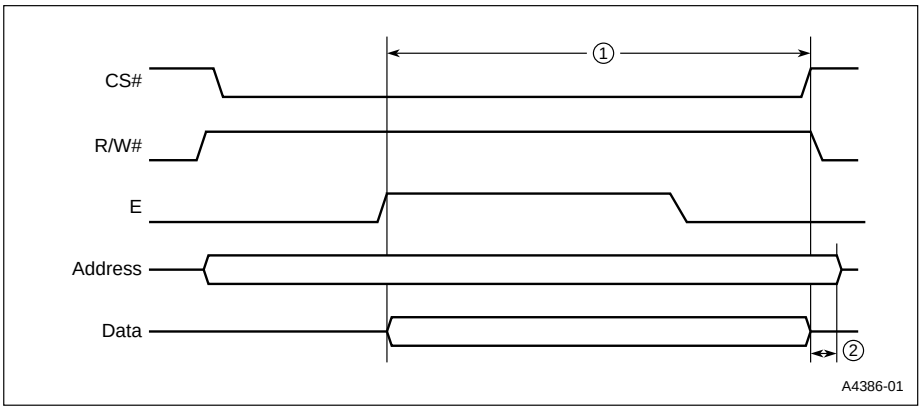


Figure 3: Bus Cycle for Mode 3 Synchronous Operation (Read Cycle)

Mode 3 asynchronous is also a demultiplexed mode of operation on the 82527. This mode is typically used with the DSACK0# signal. When using mode 3 asynchronous with host CPUs that do not have the DSACK0# input, the following considerations must be observed to prevent problems when performing reads of the 82527.

For Mode 3 asynchronous (no DSACK0#), both of the following criteria must be true:

1) The time between consecutive CS# cycles must be equal to or greater than $2\ t_{MCLK}$.

2) Address information must remain present on the bus until after CS# goes inactive.

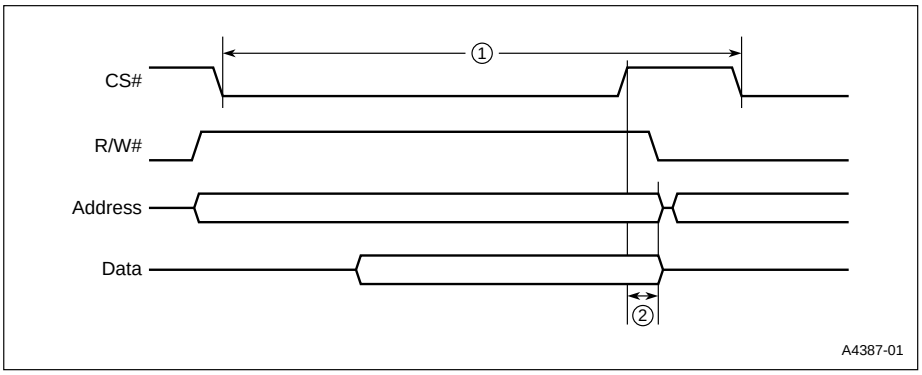


Figure 4: Bus Cycle for Mode 3 Asynchronous Operation (Read Cycle)

IMPLICATION: This problem is typically encountered when using host CPUs operating at high frequency without the capability to lengthen the bus cycle to meet the 82527's requirements for low-speed register reads. In addition, this problem is more likely to be encountered if the MCLK (memory clock) of the 82527 is configured to operate at a low frequency. The user must ensure that the above timing conditions are true in order to guarantee this undesirable behavior will not occur.

WORKAROUND: Described in prior text.

STATUS: At present, there are no plans to correct this on the 82527. The timings requirements described previously will be added to the next release of the 82527 data sheet, currently planned for Q4'96. Refer to Summary Table of Changes to determine the affected stepping(s).

SPECIFICATION CHANGES

None for this revision of this specification update.

SPECIFICATION CLARIFICATIONS

None for this revision of this specification update.

DOCUMENTATION CHANGES

None for this revision of this specification update.