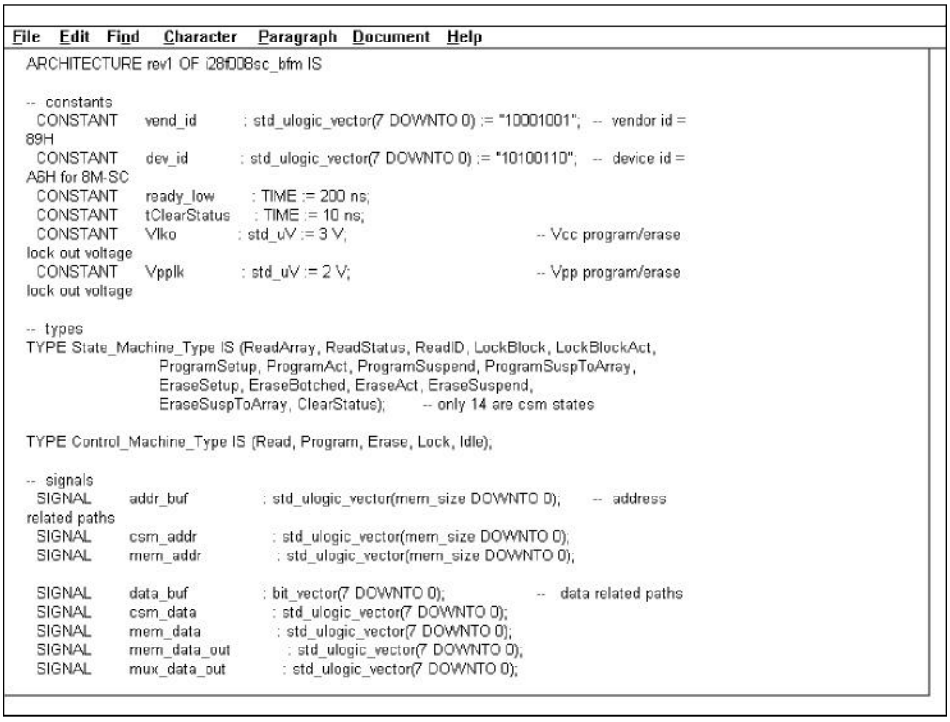
VHDL/Verilog Models

- Mimics logical behavior of flash device
- Represents device functionality, timings
- Used in system simulations
- Enables software development in advance of hardware
- Allows faster debug, time-to-market

VHDL/Verilog models are bus functional models written in hardware description language. These models mimic flash devices from a hardware perspective; one can read from, write to, and program the model, just like a real flash component. These models are designed to assist you in performing entire system simulations. By simulating an entire system before silicon samples are received, errors can be caught and fixed earlier in the design phase. This shortens your time-to-market and saves you money. Intel's models are available free of charge and cover a subset of the flash memory product line. For device models not available from Intel, please contact the Logic Modeling Group of Synopsys.



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```
ARCHITECTURE rev1 OF i28f008sc_bfm IS

-- constants
  CONSTANT    vend_id        : std_ulogic_vector(7 DOWNTO 0) := "10001001";  -- vendor id =
89H
  CONSTANT    dev_id         : std_ulogic_vector(7 DOWNTO 0) := "10100110";  -- device id =
A6H for 8M-SC
  CONSTANT    ready_low      : TIME := 200 ns;
  CONSTANT    tClearStatus   : TIME := 10 ns;
  CONSTANT    Vlko           : std_uV := 3 V;                                -- Vcc program/erase
lock out voltage
  CONSTANT    Vpplk          : std_uV := 2 V;                                -- Vpp program/erase
lock out voltage

-- types
TYPE State_Machine_Type IS (ReadArray, ReadStatus, ReadID, LockBlock, LockBlockAct,
                    ProgramSetup, ProgramAct, ProgramSuspend, ProgramSuspToArray,
                    EraseSetup, EraseBotched, EraseAct, EraseSuspend,
                    EraseSuspToArray, ClearStatus);       -- only 14 are csm states

TYPE Control_Machine_Type IS (Read, Program, Erase, Lock, Idle);

-- signals
  SIGNAL      addr_buf             : std_ulogic_vector(mem_size DOWNTO 0);     -- address
related paths
  SIGNAL      csm_addr             : std_ulogic_vector(mem_size DOWNTO 0);
  SIGNAL      mem_addr             : std_ulogic_vector(mem_size DOWNTO 0);

  SIGNAL      data_buf             : bit_vector(7 DOWNTO 0);                   -- data related paths
  SIGNAL      csm_data             : std_ulogic_vector(7 DOWNTO 0);
  SIGNAL      mem_data             : std_ulogic_vector(7 DOWNTO 0);
  SIGNAL      mem_data_out         : std_ulogic_vector(7 DOWNTO 0);
  SIGNAL      mux_data_out         : std_ulogic_vector(7 DOWNTO 0);
```

INTEL FLASH MEMORY SUPPORTED:

VHDL: 28F004SC, 28F008SC, 28F016SC, 28F016SV, 28F016XD, 28F016XS

Verilog: 28F400BV, 28F008SA, 28F800BE, 28F800BV, 28F800CE, 28F016SA

Note: As additional models become available, Intel will add them to the WWW and BBS.

AVAILABILITY:

Now

CONTACT:

See Appendix C