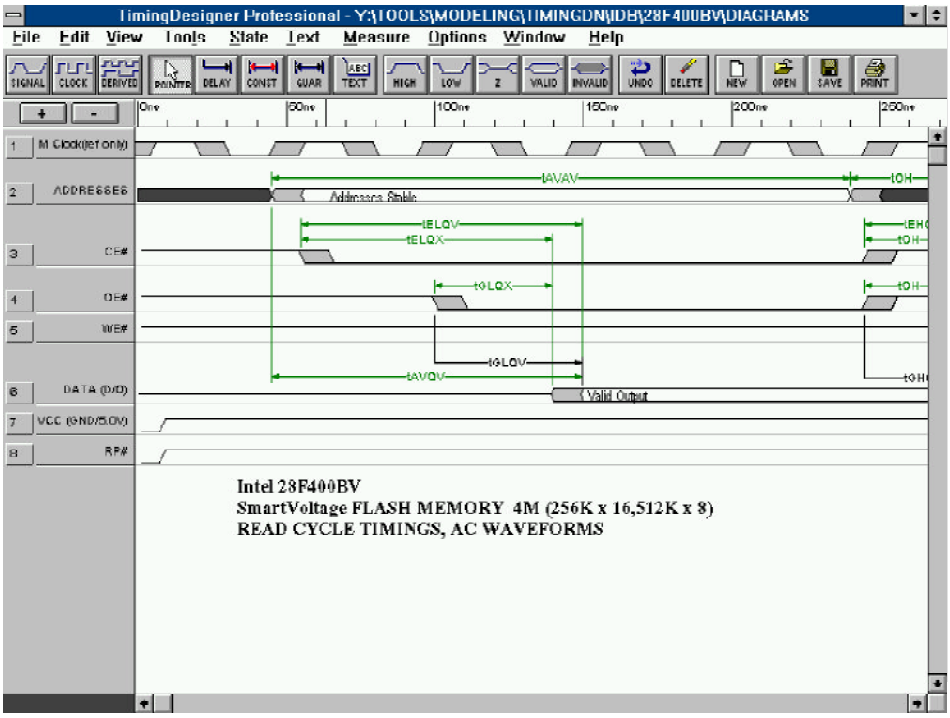
TimingDesigner* Models

- Device read/write timing models
- Enables interface timing analysis in design
- Ensures timing compatibility between memories, microprocessors, programmable logic, etc.
- Runs under Chronology's TimingDesigner*/TimingViewer*

TimingDesigner models are interactive databooks, which are electronic timing diagrams that are viewed and manipulated on the computer. They are used for interface timing analysis in a system design and aid in choosing the appropriate system components or parameters. TimingDesigner models help to ensure timing compatibility between devices. These files are created by Intel but operate under TimingDesigner and TimingViewer, both by Chronology Corporation. TimingDesigner models and TimingViewer are both available from Intel, free of charge.



INTEL FLASH MEMORY SUPPORTED:

28F010, 28F001BX, 28F020, 28F002BC, 28F002BL, 28F002BV, 28F002BX, 28F200BL, 28F200BV, 28F200BX, 28F200CV, 28F004BE, 28F004BL, 28F004BV, 28F004BX, 28F004SC, 28F400BL, 28F400BV, 28F400BX, 28F400CE, 28F400CV, 28F008BE, 28F008BV, 28F008SA, 28F008SC, 28F800BV, 28F800CE, 28F800CV, 28F016SA, 28F016SC, 28F016SV, 28F016XD, 28F016XS, 28F032SA

Note: As additional models become available, Intel will add them to the WWW and BBS.

AVAILABILITY:

Now

CONTACT:

See Appendix C

* Other brands and names are the property of their respective owners.