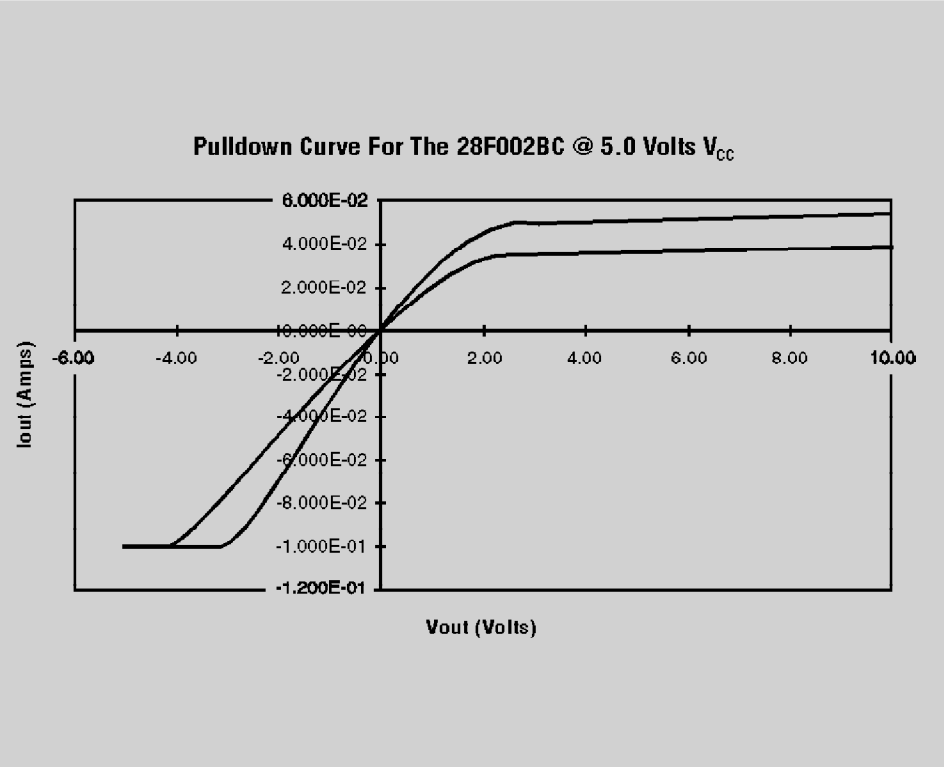
IBIS Models

- Model the analog characteristics of I/O buffers
- Used to perform PCB interconnect simulations
- Resolves compatibility issues when upgrading devices
- Can be imported into SPICE



An IBIS (I/O Buffer Information Specification) model is a behavioral description of the I/O buffers and packaging electrical characteristics of a flash device. These models provide information such as I/V curves, package characteristics, and rise/fall times, all measured at various voltages and temperatures. IBIS models present the electrical characteristics of the input, output, and I/O buffers without revealing the underlying proprietary transistor or process information. They are used in PCB interconnect simulations to determine electrical stability of high-speed buses. These models help to resolve issues revolving around the analog behavior of flash memory components, such as overshoot, undershoot, ringing or transmission line effects. They are especially useful when converting between flash memory devices which may have different electrical characteristics, such as process steppings. IBIS models can be used in SPICE simulators by importing the ASCII IBIS text file into SPICE. These models have passed the Golden Parser and are available free of charge from Intel, who bases these models on actual device lab measurements, not simulation results.

INTEL FLASH MEMORY SUPPORTED:
28F001BX, 28F002BC, 28F002BL, 28F002BV, 28F002BX, 28F200BL, 28F200BV, 28F200BX, 28F200CV, 28F004BE, 28F004BL, 28F004BV, 28F004BX, 28F004SC, 28F400BL, 28F400BV, 28F400BX, 28F400CE, 28F400CV, 28F008BE, 28F008BV, 28F008SA, 28F008SC, 28F800BV, 28F800CE, 28F800CV, 28F016SA, 28F016SC, 28F016SV, 28F016XD, 28F016XS, 28F032SA

AVAILABILITY:
Now

CONTACT:
See Appendix C