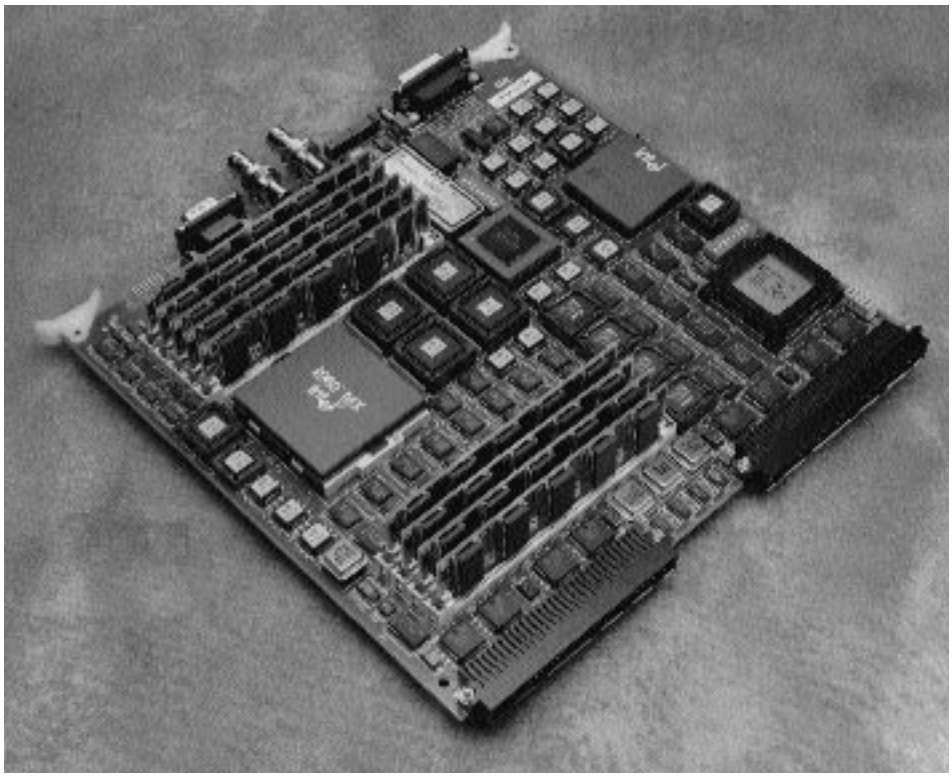
PI960MX-JXV JIAWG Execution Vehicle

- i960® MM/MX Processor 20 MHz Board Design With Extended or Protected Mode Support
- Dual Pi Bus Backplane Interfaces
- Dual MIL-STD-1553B Interfaces
- IEEE 802.3 Ethernet Interface (Optional)
- RS-232 Serial Interface
- 1 to 4 Mbytes of 64-Bit + Tag Backside Bus SRAM
- 1/2 to 4 Mbytes of 33-Bit Local Bus SRAM
- 1 Mbyte of Flash EPROM
- Flash EPROM-Resident Monitor and Diagnostics
- 82C54 Programmable Timer/Counter
- 6U x 220mm Eurocard Form Factor
- i960 Processor ICE Bus Interface



The PI960MX-JXV features Intel's super-scalar microprocessor chosen by JIAWG as a 32-bit processor standard. The i960 MM/MX processor can decode and execute multiple instructions per clock cycle, resulting in a performance greater than 20 million instructions per second at 20 MHz.

The base configuration of the PI960MX-JXV includes one Mbyte of zero wait state SRAM on the backside bus and a half Mbyte of SRAM on the local bus. Cache control logic maintains coherency between the backside memory and the local memory. Both backside and local memory structures are expandable to four Mbytes to better fit your application. This flexible memory structure makes the PI960MX-JXV ideal for benchmarking or evaluating the performance of your application software.

Multiple Interface Execution Vehicle
The PI960MX-JXV is designed for ease of use in numerous environments. Dual Pi Bus interfaces provide high performance board to board communications across the JIAWG standard backplane. An optional MIL-STD-1553B serial interface can be added, yielding additional development capabilities and providing the means to interface to your existing hardware. The PI960MX-JXV also features an RS-232 serial interface and an Ethernet interface for communicating with your host system. In addition, access to the i960 MM/MX processor ICE bus is provided for added capabilities in debugging your software.

Software Development Environment
As the first i960 MM/MX processor based execution vehicle, the PI960MX-JXV will support your early application software development and debug efforts. Several third party Ada vendors support the PI960MX-JXV.

PROCESSORS SUPPORTED:
i960 MM/MX Processors

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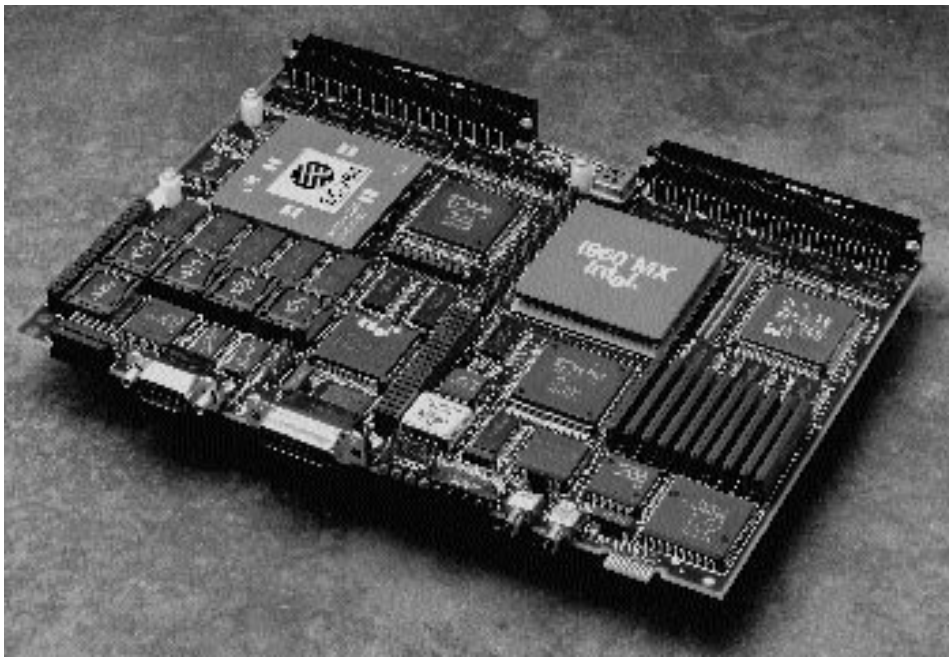
VME960MX-SBC and VME960MC-SBC Single-Board Computers

- Supports the i960® MX/MM or MC/XA Processors in Extended or Protected Mode
- VMEbus 64-Bit Interface (IEEE 1014 Rev D, Master/Slave Capable)
- 1 or 3 Mbytes of 64-Bit + Tag Backside SRAM (VME960MX-SBC Only)
- 4 Mbytes of DRAM and 1/2 Mbyte of SRAM on the System Bus, Both 33-Bits Wide
- 1 Mbyte of Flash EPROM With Resident Monitor and Diagnostics
- IEEE 802.3 Ethernet Interface, Two RS-232 Serial Interfaces, One Parallel Port
- MIL-STD-1553B Capable (VME960MC-SBC Supports Dual-Dual MIL-STD-1553B)
- Five Programmable Timer/Counters
- Battery Backed Time-of-Day Clock and Calendar
- Versatile I/O Adaptor Interface Supports User Defined Daughter Cards



The VME960MX-SBC features Intel's 20 MHz i960 MX/MM superscalar microprocessor, the newest member of Intel's military family of i960 embedded microprocessors. Using advanced RISC technology and five parallel execution units, the i960 MX processor is capable of executing up to three instructions per clock, resulting in a performance greater than 20 million instructions per second at 20 MHz.

Reliable i960 MC/XA Processor Performance

The VME960MC-SBC features Intel's highly integrated i960 MC/XA RISC microprocessor. The board and processor operate at 25 MHz and support both the i960 MC/XA processor modes of operation. An industry workhorse, the i960 MC/XA processor has hundreds of design wins to date. It too implements the JIAWG 32-bit instruction set architecture when operating as an i960 XA processor, and uses a 33rd tag bit to support object-oriented programming and data security. With on-chip virtual-memory management, floating-point arithmetic, and multi-tasking capabilities, the i960 MC processor provides sustained instruction execution rates of 10 MIPs.

Common Architectures

Tronix's VME960 single-board computers have a flexible, user configurable memory structure. The backside resident memory of the VME960MX-SBC can be 1 or 3 Mbytes of zero wait state, 64-bit SRAM that also supports Tag bits. It can be configured as cache or private memory, depending on your application. The system bus memory, common to both boards, is 4 Mbytes of 33-bit DRAM and 1/2 Mbyte of 33-bit SRAM. Its control logic supports programmable wait states for evaluating the effects of slower memory on your application software.

Flexible I/O Structure

Both VME960 single-board computers implement an IEEE 1014 (Rev D) VMEbus interface using the Newbridge SCV64. 64-bit data transfers are possible at speeds up to 70 Mbytes/sec. in MBLT mode, allowing you to take full advantage of the i960 microprocessors.

I/O features common to both include an IEEE 802.3 Ethernet interface using Intel's 82596CA, two RS-232 serial ports, a parallel port, and an optional MIL-STD-1553B interface. Also, a versatile I/O adaptor interface permits on-board configuration with user defined daughter cards — allowing you to make the choice.

PROCESSORS SUPPORTED:
i960 MX/MM/MC/XA Processors

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