V960xPBC Family PCI Local to PCI Bridge Controllers

- Glueless Interface Between Intel's i960® Embedded Processors and the Industry Standard PCI Bus
- Fully Compliant With PCI 2.1 Specification, Windows95 and WindowsNT
- 576-bytes of Programmable FIFO Storage With *Dynamic Bandwidth Allocation**
- Configurable For System Master, Bus Master or Target Operation
- 1 Kbyte Burst Access Support on Both Local, and PCI Interfaces
- Optional Power-on Configuration Through Serial EEPROM
- Two Channel DMA Controller With Chaining
- Integrated Bidirectional Mailbox Registers
- Local-to-PCI and 2 PCI-to-Local Address Apertures
- On-the-Fly Byte Order (Endian) Conversion
- Real Mode DOS Support

Typical Application

The V96xPBC family provides a flexible, high performance and economical way to connect i960 embedded processors to the PCI bus. The V96xPBC has been designed in compliance with the PCI2.1 specification as well as the special requirements for Windows95/NT compatibility.

The V96xPBC supports independent interface speeds, allowing the PCI bus to run at the full 33 MHz frequency, regardless of processor clock rate. The unique *Dynamic Bandwidth Allocation** feature of the 576 byte FIFO's allows the designer to adjust the "draining" and "filling" of the read and write FIFO's to most efficiently meet the requirements of the data streams. Inclusion of this large FIFO array insures that high-speed peripherals – such as ATM and 100 Mbit Ethernet adapters – won't overrun the bridge's buffering capability.

The on-chip 2 channel DMA controller allows for scatter/gather operation and enables unattended transfers between PCI devices and local memory.The i960 family of processors gain access to the PCI bus through two programmable address apertures. Two additional apertures are provided for PCI-to-local bus accesses. The V96xPBC's include bidirectional address remapping capabilities that allow PCI addresses to be remapped into another region of the local address space and visa-versa. In addition, the V96xPBC family provides on-the-fly byte order (endian) conversion.

Programmable configuration space registers allow V96xPBC systems to comply with PCI auto-configuration guidelines. The integrated mailbox registers provide a simple mechanism to emulate PCI device control ports. The V96xPBX device programming registers are accessible through the host interface, through the PCI interface, or through a power-on serial EEPROM configuration port. The V96xPBC family are available in 16, 20, 25, 33 & 40 MHz versions and are packaged in low cost 160-pin EIAJ PQFP.

PROCESSORS SUPPORTED:
i960 Cx, Kx, Sx, Jx, Hx Processors

AVAILABILITY:
Samples 8 wks ARO; 9/15/95 production

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