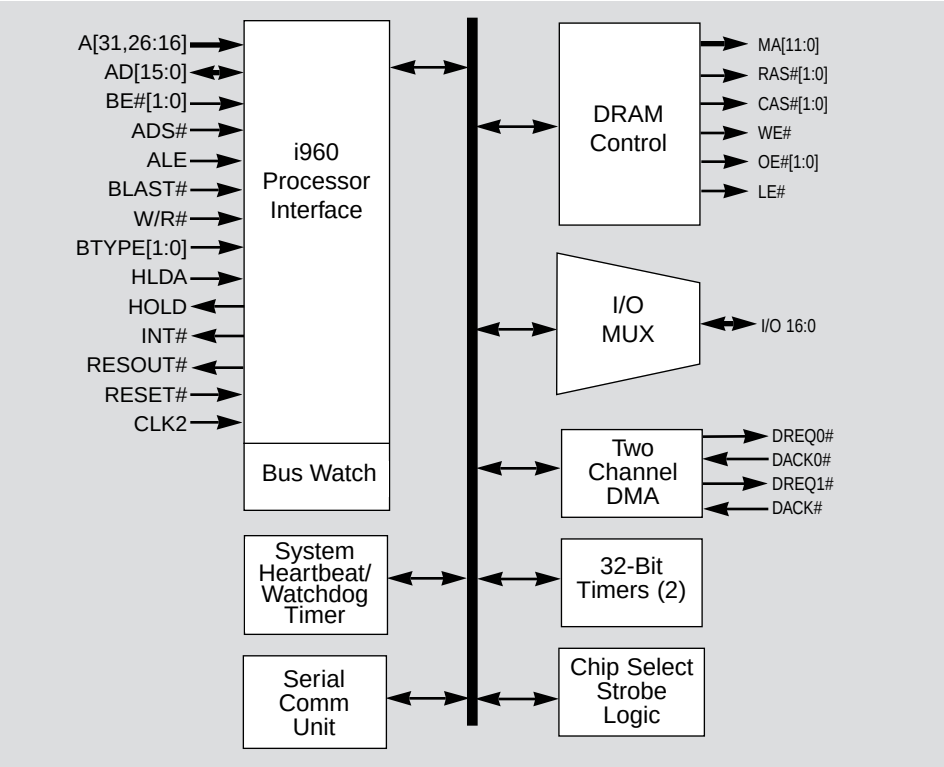
V96SSC High-Integration Controller

- Glueless Interface to Intel's i960® Sx and i960 Jx Series Processors
- High-Performance DRAM Controller With DRAM Page Cache Management and EDO Support
- Two Channel Fly-By DMA Controller
- Synchronous/Asynchronous Serial Communication Unit
- Programmable Chip Select/ Peripheral Device Strobe Generation
- Programmable System Heartbeat and System Watchdog Timers
- Two 32-Bit General Purpose Timers With Pulse Width Modulation Capability
- General Purpose Bit I/O Ports
- Interrupt Control Unit
- Fastest Time-to-Market For i960 Sx and i960 Jx Series Microprocessor Designs



Typical Application

The V96SSC High-Performance System Controller is a single-chip device that simplifies the design of systems based on Intel's i960 Jx and i960 Sx series embedded microprocessors. By using the V96SSC, system designers can replace many lower integration support components with a single high-integration device; saving design time, board area and manufacturing cost.

The integrated DRAM controller directly connects the i960 family processors to DRAM arrays from 128 KB to 64 MB. The DRAM controller is fully programmable, allowing the use of a wide range of DRAM speeds and configurations including EDO DRAMS. Burst accesses are supported up to 256 transactions in length, allowing for the use of high-performance bus-mastering peripherals.

The two channel fly-by DMA controller makes it easy to use less expensive, non-mastering peripherals in your system. To further aid in connecting the i960 processor, the V96SSC's I/O Controller performs address decoding and chip-select/strobe generation. In addition, the I/O lines may be used as simple I/O ports on a bit-by-bit basis. An on chip serial communications unit is also provided for connecting to either RS-232 or synchronous serial devices.

The two general purpose 32-bit timers may be configured as a pulse width modulator or used separately in either retriggerable or one-shot modes. The bus watch timer prevents system hangs during accesses to unpopulated memory. Interrupts for a real time OS can be easily generated by the system heartbeat timer. A watchdog timer is also provided for graceful recovery from software upsets.

Interrupt requests for all on-chip peripherals are managed by the interrupt control unit. Additionally, off-chip interrupts can be routed to the interrupt control unit via the I/O multiplexer. The V96SSC is packaged in a low-cost 100-pin EIAJ PQFP in 16, 20, and 25 MHz versions.

PROCESSORS SUPPORTED:
i960 Sx/Jx Processors

AVAILABILITY:
Sampling now; 9/15/95 production

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