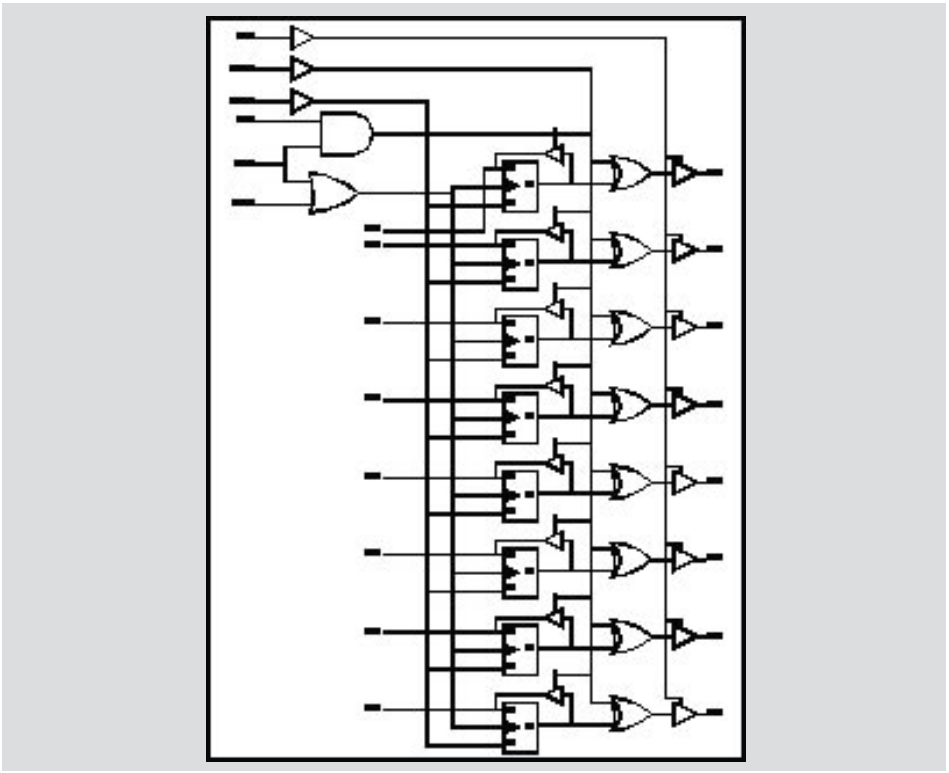
DM74ALS996 Edge-Triggered Readback Latches

- Supports All i960® Processors
- TRI-STATE I/O-Type Read-Back Inputs
- TRI-STATE Bus-Driving Outputs
- Bus-Structured Pinout
- True or Complementary Data at Q Outputs
- Ideal For Applications Such As Setup Registers, Redundancy, Self-Diagnostics



These 8-bit registers are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto that bus. The Q output are designed with bus driving capability.

The edge-triggered flip-flops enter the data on the low-to-high transition of the clock (CLK) when enable (WR) is low. Data can be read-back onto the data inputs by taking the read input (RD) low, in addition to having WR low. Whenever WR is high, both the read-back and write modes are disabled. Transitions on WR should only be made with CLK high in order to prevent false clocking.

The polarity of the Q outputs can be controlled by the polarity input PRY. When PRY is high, Q will be the same as is stored in the flip-flops. When PRY is low, the output data will be inverted. The Q outputs can be placed into Tristate by taking the output control (OC) high. The output control OC does not effect the internal operations of the register. Old data can be retained or new data can be entered while the outputs are off.

A low level at the clear input (CLR) resets the internal registers low. The clear function is asynchronous and overrides all other register functions.

PROCESSORS SUPPORTED:
i960 Processor Family

AVAILABILITY:
Now

CONTACT:
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For international contacts see Appendix B.

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