

S44XX Clock Generators

- Generate Multiple TTL Clock Outputs From 20 MHz to 80 MHz
- Controlled Edge Rate TTL Outputs Have Less Than 400 ps of Skew
- Support Clock Doubling, Dividing, Invert and Lead/Lag Functions
- Internal Phase Locked Loop (PLL) With VCO Operating at 160 to 320 MHz

System design based on the i960[®] micro-processor often requires multiple frequencies or phases of the reference clock to maintain optimum speed while minimizing the effects of skew, bus timing and EMI. AMCC has developed the S44XX family of clock generators to assist high-performance designers in the generation and synchronization of multiple clocks in their system.

The S4402 and S4403 devices provide up to six and 10 outputs, respectively, which can be configured to provide 21 different phase and frequency relationships. Each has an on-chip Phase Locked Loop (PLL), which is used to generate TTL outputs from 10-80 MHz when locked to a reference frequency between 20 and 80 MHz. Each output is guaranteed to be skewed ≤ 400 ps from any other output. The outputs can be programmed using a bank of control pins to produce signals that are 2x or 1/2x the "primary" output frequency. The output phase can also be modified to generate leading or lagging clocks.

The S4405 is functionally equivalent to the S4403 with the addition of 5 V positive-referenced differential ECL (PECL) input and one differential PECL output. This device is ideal for systems based on the i960[®] microprocessor that use a high-speed, low noise PECL back-plane.

The S4406 provides 12 TTL outputs grouped as four banks of three outputs. Each bank can be individually programmed to generate outputs at 2x, 1/2x

Clock Generator/Synthesizer Selection Guide					
Part	Description	Input Reference	No.	Type	Max. Out Freq.
S4402	Multiphase Clock Generator	TTL	6	-	100
S4403	Multiphase Clock Generator	TTL	10	-	100
S4405	Multiphase Clock Generator with PECL In	PECL/TTL	6	PECL	100 150
S4406	Clock Generator with Delay Adj. & Invert	TTL	12	-	100
S4407	Clock Multiplier	TTL	2	-	130
S4408	Deep Synthesizer	XTAL	2	PECL	100 130
Full Family	3.0V Clock Generator with Delay Adj. & Invert	LVCMOS	12	LVCMOS	80

or 1x the primary output frequency. The banks can also be configured to lead or lag the phase of the other outputs.

PROCESSORS SUPPORTED:
i960[®] Processor Family

AVAILABILITY:
Production quantities available now

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For international contacts see Appendix B.