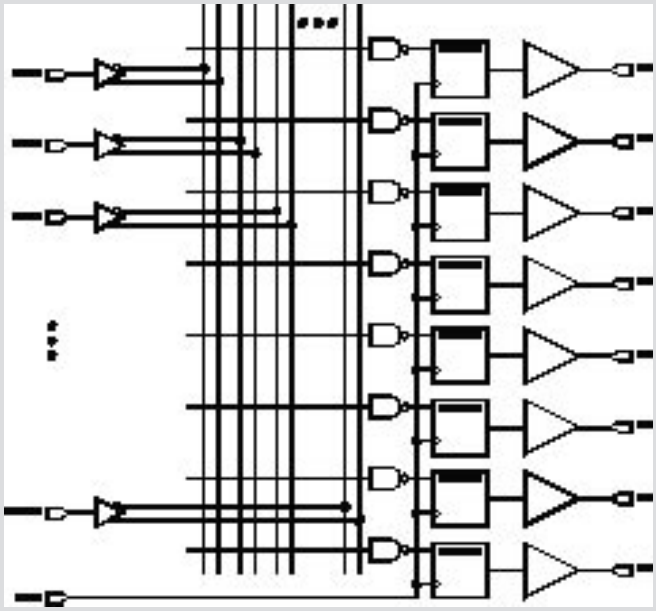
85C508 High Address Decoder

- High-Speed Address Decode For High-Performance Designs
- Wide Address Decode – 16 Inputs
- Up to 8 Chip-Select Outputs
- Low-Power CHMOS Technology
- Total Propagation Delay of 7.5 nsec (Maximum)



The 85C508 offers high-speed address decode for i960® CA/CF processor systems. The 85C508 decodes 16 address inputs into 8 chip-select outputs. The chip selects may be latched if desired. Total propagation delay for the device is 7.5 nsec maximum. Power consumption is 48 mA maximum due to low-power CHMOS technology. The 85C508 is housed in 28-pin, 300-mil ceramic DIP and plastic DIP packages, or 28-pin PLCC package for surface mount. In the CerDIP package, the device is UV erasable and reprogrammable.

PROCESSORS SUPPORTED:
i960 CA/CF Processors

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