PCI PLX TECHNOLOGY

## PCI 9060

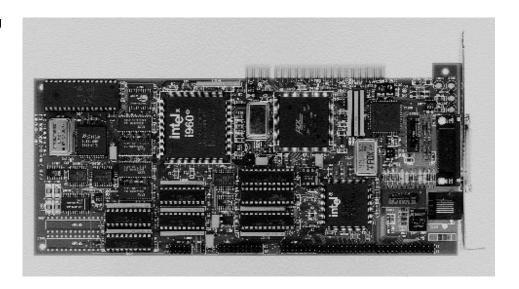
- PCI Bus Master Interface Supporting i960® Microprocessor Based Adapters and Systems
- Two Independent DMA Channels
  For Local Bus Memory to PCI Host
  Bus Data Transfers
- Four Bidirectional FIFOs For Zero Wait State Burst Operation; One For Each DMA Channel, Direct Master Interface and Slave Interface
- PCI Bus Master Transfers Up to 132 Mbytes/sec.
- Direct Connect to 80960 Local Bus;
  Cx, Hx, Jx, Kx, Sx, Single or Multi-Local Bus Configurations
- Eight 32-Bit Mailbox and Two 32-Bit Doorbell Registers
- Low Power CMOS in 208-Pin Plastic QFP Package

PLX delivers low cost, highly integrated PCI connections to I/O adapters such as RAID, SCSI and LAN plus embedded systems such as switching hubs, routers and printers. PLX's PCI 9060 series is a family of three interface chips that serve applications ranging from low cost slave adapters to high performance intelligent adapters and embedded systems.

In adapter applications, the PCI 9060 chips provide high speed data transfer between the host system and the adapter's local bus. The PCI 9060 also generates the PCI bus for embedded systems, many of which are starting to employ PCI instead of a proprietary bus. All three chips in the family have direct interfaces to the i960 processors.

## **PCI 9060 Features and Applications**

The flagship product of the series, the PCI 9060, is targeted to adapters and embedded systems based on Intel's i960 microprocessors. The PCI 9060 provides all the logic required for a complete high performance PCI interface. A two channel chaining DMA controller enables 132 Megabyte/second transfers between the adapter or embedded system local bus and the PCI bus, even when the local bus runs



at a speed slower than the 33 MHz PCI. Each channel contains a bidirectional FIFO to enable zero wait state burst transfers across the PCI bus. The DMA controller is compatible with the Intel i960 processor family DMA, which makes programming simple. A separate direct master channel with a bidirectional FIFO allows the CPU or I/O controllers to become masters on the PCI bus for minimum latency data or command transfers. Mailbox and doorbell registers provide a means for message passing and interrupt generation. The PCI 9060 is programmable to three local bus modes providing a glue-less interface to the i960 Cx, Hx, Jx and Sx processors.

## PCI 9060SD and PCI 9060ES

For lower cost applications, PLX offers two-feature reduced versions of the PCI 9060, and PCI 9060SD and PCI 9060ES. Both are 100% pin and software compatible with the PCI 9060, providing product scalability advantages.

CONTACT:

Mike Hopwood PLX Technology 625 Clyde Avenue Mountain View, CA Phone: (415) 694-2800

Phone: (415) 694-2800 FAX: (415) 960-0479

e-mail: PLX@NETCOM.COM

