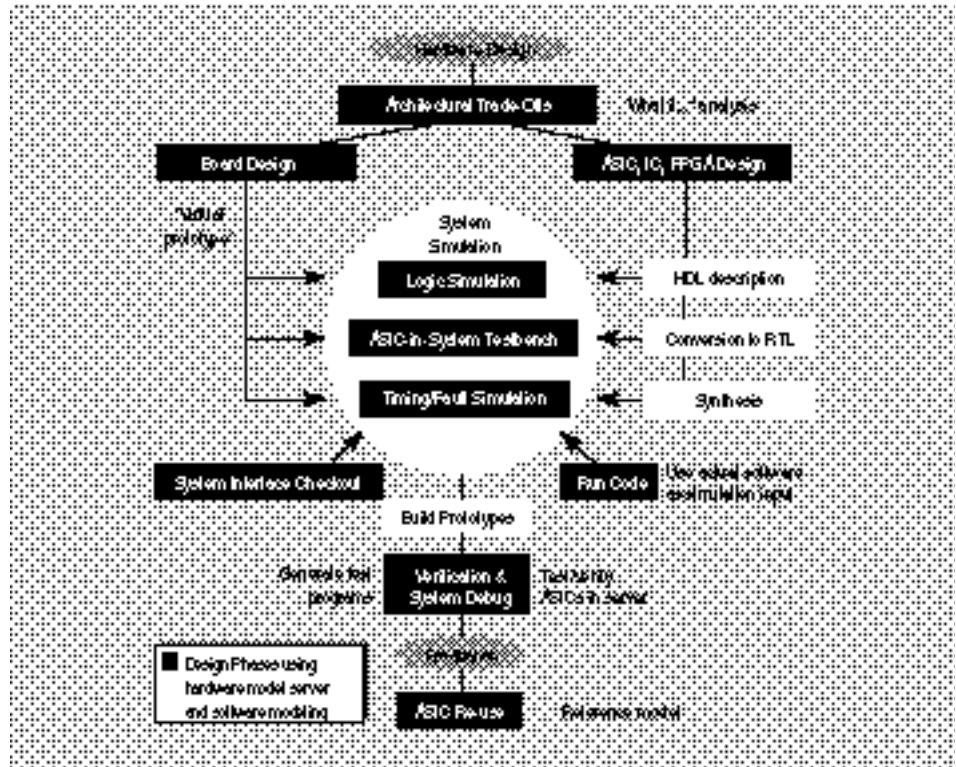# Simulation Models

- Comprehensive Approach to Simulation Modeling Needs
- Broadest Device Coverage: Microprocessors, FPGAs, PLDs, DSPs, Logic and Memories
- Early Model Availability, Some Models Available Pre-Silicon
- All Models Have Intelligent Error Checking, Full-Timing, and Consistent Unknown Handling to Improve Simulation Accuracy

Logic Modeling—through its ModelSource* and LM-family* of hardware modelers, SmartModel* Library and the VHDL SourceModel* Libraries—provides board, system and ASIC designers with a comprehensive solution to their simulation model needs.

The ModelSource 3000 series and the LM-family hardware model server brings the benefits of hardware modeling—accuracy, fully-functional behavior, easy model development, and excellent simulation performance—to the desktop. They use the actual physical device to model its own behavior during simulation. As a result, hardware models always provide accurate and full device functionality, including any undocumented behavior. With hardware models, designers can execute actual code during simulation, improving design verifications and accelerating software integration and debug. In addition to over 600 models available from Logic Modeling, ModelTools* model development software allows designers to quickly develop their own hardware models, usually in a matter of days.

The SmartModel Library contains models of more than 8,000 components from more than 40 semiconductor companies. Devices supported include microprocessors, DSPs, PLDs, memories and FPGAs.

SmartModels offer expert assistance to the board designer. Each model performs a series of usage and timing checks during simulation that look for undefined inter-

rupts, uninitialized registers, illegal conditions or any misuse of the component that is likely to slow or stall the design process. Any errors that are discovered are thoroughly documented, with the part instance, pin name and time of occurrence specified.

The VHDL SourceModel Libraries are accurate, behavioral-level models of over 3,400 of the most needed standard logic and memory components used in board-level design today. The models are written and distributed in VHDL source code format for maximum flexibility and ease-of-use. Full device functionality and timing are modeled with intelligent error checking to immediately alert the user to potential timing or usage violations.

Logic Modeling's bus interface models allow a designer to verify a designs compliance to a particular bus specification by emulating the behavior of the rest of the system and monitoring bus activity for protocol compliance.

SUPPORT AND AVAILABILITY:
Products and worldwide support are available directly from the Logic Modeling Group

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